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Bridge ASIC Datasheet

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1. Overview

This specification explains the request items of BridgeASIC as electrical characteristics and so on.

1) Supply Voltage

Core Voltage	: 1.1V (Typ)
IO Voltage	: 1.8V (Typ)
OTP Voltage	: 3.3V (Typ)

2) Current

Active	: 40mA
Standby1	: 30mA
Standby2	: 20mA
Sleep	: 2mA

3) Interface

Host Interface	: eMMC I/F (JEDEC Standard Rev4.5 compliance) for HOST SoC
Memory Interface	: 8bit I/O Nintendo Custom Interface for Memory

4) Performance

Transfer Rate	: 100MByte/sec (SoC I/F) 66MByte/sec (MAX) (Memory I/F)
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5) Security

Host Interface	: Mutual authentication and Data encrypted
Memory Interface	: Support T1/T2 Security protocol

6) Embedded IP

CPU	: Coretex-M3 (ARM)
PLL	: MegaChips Original IP. Support SSCG
Memory	: OTP 2KByte (Kilopass) SRAM (TSMC) Total 41.75KByte ROM (TSMC) Total 4KByte
Rand generator	: MegaChips Original

7) Package CSP48

2. General Description

Bridge ASIC issue command and execute data access to Memory Card by ordering from Host SoC.

Between Host SoC and this ASIC, eMMC protocol is used.

At first between Host SoC and this ASIC, mutual authentication is executed, and data is encrypted

This ASIC supports T1/T2 security protocol of Memory interface.

This ASIC has microprocessor (Coretex-M3) and firmware is transferred from Host SoC.

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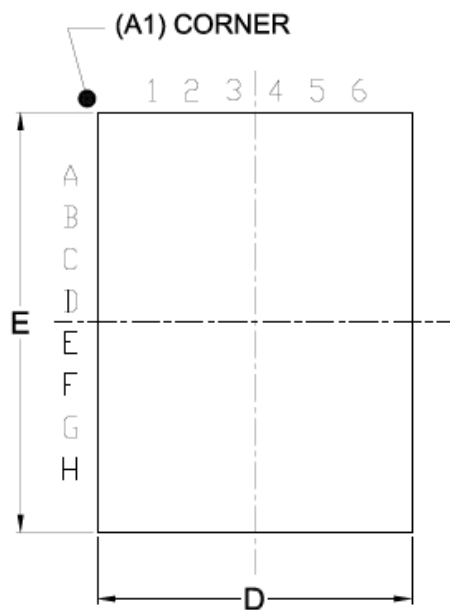
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3. Pin Configurations

Table 1. Pin Assignment (CSP48)

	1	2	3	4	5	6
A	GND	E_DAT0	E_DAT2	C_IO7	VDDIO_OTP	GND
B	E_CLK	E_DAT1	GND	C_IO6	C_RESB	GND
C	E_RESB	VDDPST	E_DAT3	C_IO4	C_IO5	VDDPST
D	GND	GND	E_CMD	C_IO2	C_IO3	C_CEB
E	CVDD	E_DAT7	E_DAT6	C_IO1	GND	C_CLK
F	XIN	VDDPST	E_DAT4	C_IO0	CVDD	VDDPST
G	XOUT	GND	E_DAT5	C_DQS	TST1	GND
H	GND	AVDD_KDFS	GND	GND	C_DET8	GND

TOP VIEW



BOTTOM VIEW

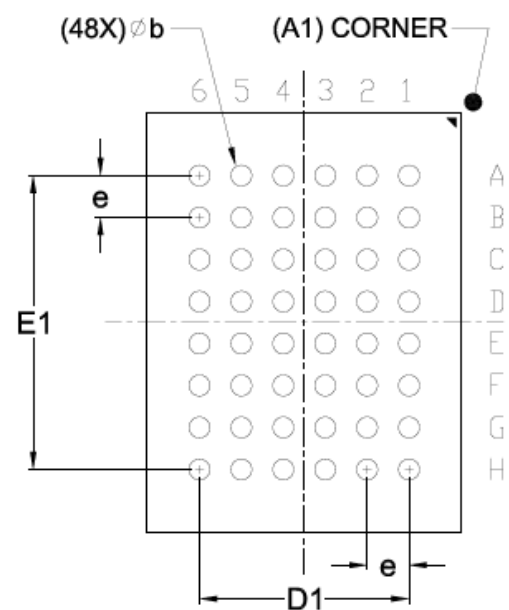


Figure 1. Pin Location (CSP48)

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4. Pin Description

Table 2. Pin Description

Terminal Name	In/Out	Pull-up/ Pull-Down	Schmitt	Explanation
XIN	I	-	-	OSC Input (25MHz)
XOUT	O	-	-	OSC Output
E_RESB	I	-	Schmitt	System Reset From Host CPU
E_CLK	I	-	-	eMMC Clock 100MHz (Max)
E_CMD	I/O	-	Schmitt	eMMC Command
E_DAT	I/O	-	Schmitt	eMMC Data I/O
C_CEB	O	-	-	Memory Chip Enable
C_RESB	O	-	-	Memory Reset
C_CLK	O	-	-	Memory Clock 66MHz (Max)
C_IO	I/O	Pull-up	Schmitt	Memory Data I/O
C_DQS	I	Pull-up	-	Memory Data Strobe
C_DETB	I	Pull-up	Schmitt	Memory Card detect
TST1	I	Pull-down	-	For TEST
VDDIO_OTP	P	-	-	3.3V Power supply for OTP
VDDPST	P	-	-	1.8V Power supply for I/O
CVDD	P	-	-	1.1V Power supply for Core
AVDD_KDFS	P	-	-	1.1V Power supply for PLL
GND	G	-	-	GND

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5. Block Diagram

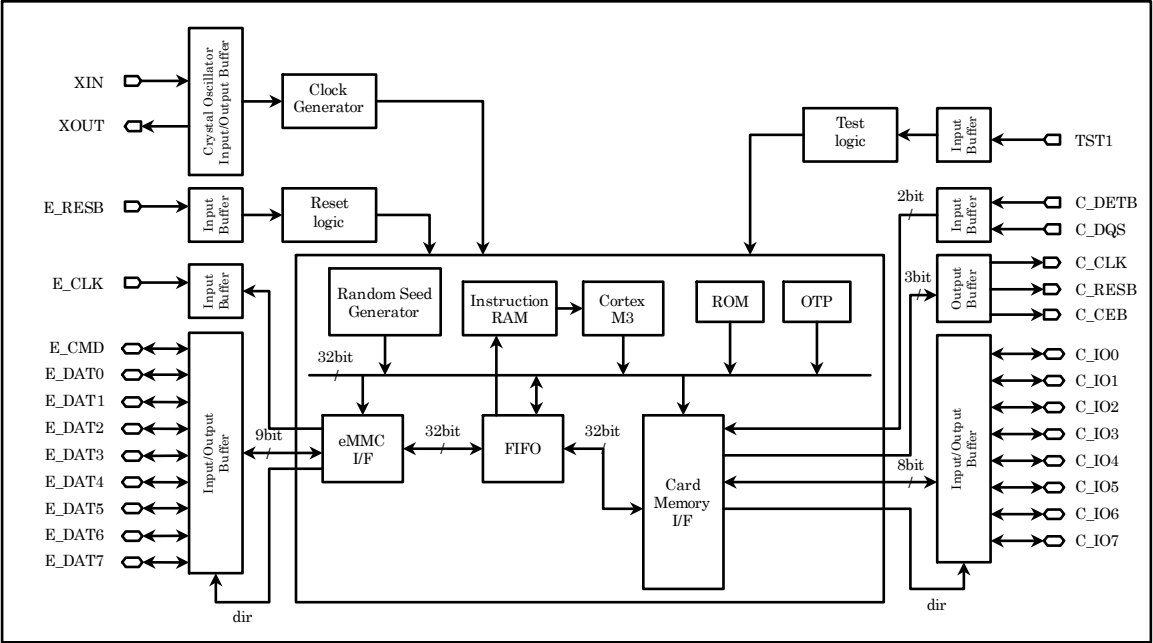


Figure 2. Block Diagram

6. OTP Memory

Table 3. OTP Memory Element Table

Item	bits	Note
UKEY1	2048	Unique Key1
UKEY2	2048	Unique Key2
UDATA	8192	Unique Data
DeviceID	128	Unique Device ID
Checksum (CRC32)	32	CRC32{UKEY1, UKEY2, UDATA, DeviceID}
PAIR_no	40	Unique ID for Manufacturing
HW Version	32	
TEST Prohibition Flag	1	
Rewind Blocked Flag	1	*1
MP/DEV	1	*1
FW Version	62	*1

*1 Refer to Table 4

Table 4. Setting Description

Rewind Blocked Flag	MP/DEV	Initial FW Version	Explanation
0	1	0	For Development (DEV)
1	0	1	For Actual Machine (STD)
0	0	0	For Verification (VAL)

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7. PLL Specification

PLL supports Spread Spectrum Clock Generator (SSCG).
Spread Spectrum mode is Down Spread (Clock Frequency is not Over the Fmax),
and Modulation Shape is Triangle Shape.

Table 5. Spread Spectrum Function

Parameter	Symbol	Min.	Typ.	Max.	Unit
Max Frequency	Fmax	-	800	-	MHz
Modulation Depth	ss_depth	-	2	-	%
Modulation Rate	ss_rate	-	82.24	-	KHz

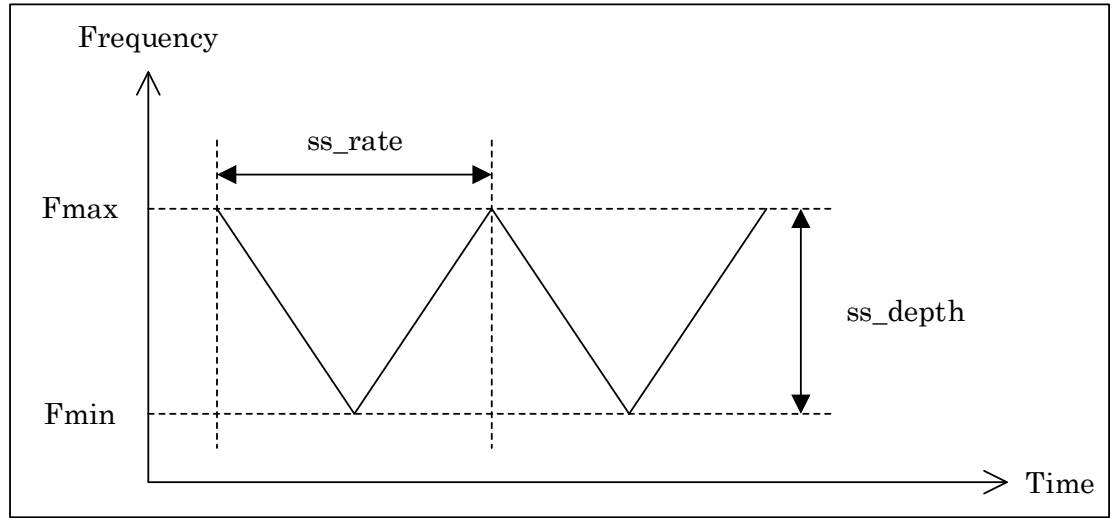


Figure 3. Frequency Modulation Profile

8. Power Up/Down Sequence

BridgeASIC requires the following power up/down sequence:

Power Up Sequence

- 1) VDDPST, CVDD and AVDD_KDFS power supply is on first
- 2) VDDIO_OTP power supply is on

Power Down Sequence

- 1) VDDIO_OTP power supply is off
- 2) VDDPST, CVDD and AVDD_KDFS power supply is off last

Table 6. Power Up/Down Sequence Spec

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power On Lag Time	tLAG1	0.1	-	500	ms
Power Up Time	tON	0.1	-	500	ms
Power Down Time	tOFF	0.1	-	500	ms
Power Off Lag Time	tLAG2	0.1	-	500	ms

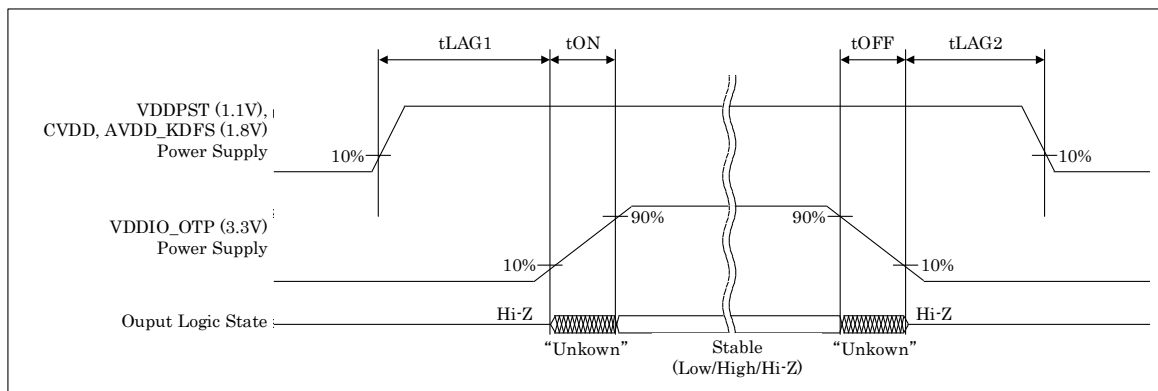


Figure 4. Power Up/Down Sequence

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9. Electrical Characteristics

9-1. Absolute Maximum Rating

Table 7. Absolute Maximum Rating

(GND=0V)

Parameter		Symbol	Rating	Unit	Condition
Supply Voltage	I/O	VDDPST	-0.5 to +4.0	V	
	OTP	VDDIO_OTP	-0.5 to +4.0	V	
	Core	CVDD	-0.5 to +1.6	V	
		AVDD_KDFS	-0.5 to +1.6	V	
Input Voltage	Standard	VIN	-0.5 to +4.0	V	
Output Voltage	Standard	VOUT	-0.5 to min (VDDPST+0.5, 4.0)	V	
DC Output Current		IOUT	±10	mA	8mA Buffer
Storage Temperature		TSTG	-55 to +125	°C	Plastic Package

9-2. Recommended Operation Condition

Table 8. Recommended Operation Condition

(GND=0V)

Parameter	Symbol	Rating	Unit
Supply Voltage	VDDPST	1.62 to 1.98	V
	VDDIO_OTP	3.00 to 3.60	V
	CVDD	0.99 to 1.21	V
	AVDD_KDFS	0.99 to 1.21	V
Operating Temperature	TA	0 to 85	°C

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9-3. DC Characteristics

Table 9. DC Characteristics

(TA = 0 ~ 85°C, VDDPST=1.8V±0.18V, CVDD=1.1±0.11V, AVDD_KDFS=CVDD=1.1±0.11V
VDDIO_OTP=3.00V ~ 3.60V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input Voltage (LVTTL)	VIH	1.17	-	-	V	
	VIL	-	-	0.63	V	
Input Voltage (Schmitt)	V+	-	-	1.3	V	
	V-	0.46	-	-	V	
Output Voltage (LVTTL)	VOH	VDDPST -0.27	-	-	V	IOH= (-4mA~-16mA) x0.3
	VOL	-	-	0.45	V	IOL= (4mA~ 16mA) x0.55
Input Leakage Current	IIH	-10	-	10	μA	VIN= VDDPST
	IIL	-10	-	10	μA	VIN= GND
Output Leakage Current	IOZ	-10	-	10	μA	Hi-Z state
Pull-up Resistor	RPU	110	194	333	kΩ	VIN= GND
Pull-down Resistor	RPD	83	159	291	kΩ	VIN= VDDPST
Operating Current	ICC_CVDD_KDFS	-	-	40	mA	
	ICC_VDDPST	-	-	30	mA	tPERIOD=10ns, tWC=20ns
	ICC_VDDIO_OTP1	-	1	1.5	mA	Read Operation
	ICC_VDDIO_OTP2	-	10	16	mA	Program Operation
Standby Current1	ICCSTB1_CVDD_KDFS	-	-	30	mA	Standby1 state
	ICCSTB_VDDPST	-	-	3	mA	E_CLK=VIH, E_CMD=VIH, E_DAT=VIH, C_CLK=VOH, C_CEB=VOH,
	ICCSTB_VDDIO_OTP	-	90	300	μA	
Standby Current2	ICCSTB2_CVDD_KDFS	-	-	20	mA	Standby2 state
Sleep Mode Current	ICCSLP_CVDD_KDFS	-	-	2	mA	Sleep state

9-4. Capacitance

Table 10. Capacitance

(TA = 0 ~ 85°C, VDDPST=1.8V±0.18V, f = 1MHz)

Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Pin Capacitance	CPIN	VOUT = 0V, VIN = 0V	-	4	pF

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10. AC Characteristic

Table 11. AC Characteristic Spec condition

Parameter		Spec Condition
Input Pulse Level		VDDPST * 0.1 to VDDPST * 0.9
Input Rise and Fall Times		1.8ns
Input Timing Level	E_CLK, E_RESB, E_CMD, E_DAT7-0	VDDPST * 0.5
	C_DQS, C_IO7-0	0.45V to VDDPST - 0.45V
Output Timing Level	E_CMD, E_DAT7-0, C_CLK	VDDPST * 0.5
	C_RESB, C_CEB, C_IO7-0	VDDPST * 0.3 to VDDPST * 0.7
Output Load	E_CMD, E_DAT7-0	15pF
	C_CLK, C_RESB, C_CEB, C_IO7-0	25pF
Supply Voltage	VDDPST	1.62 to 1.98V
	VDDIO_OTP	3.00 to 3.60V
	CVDD	0.99 to 1.21V
	AVDD_KDFS	0.99 to 1.21V
	GND	0V
Operating Temperature		0 to 85°C

10-1. eMMC Interface

10-1-1. Clock Timing

Table 12. eMMC Interface Clock signal timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	tPERIOD	10	-	-	ns
Clock High Transfer Time	tTLH	-	-	1.0	ns
Clock Low Transfer Time	tTHL	-	-	1.0	ns
Clock Cycle Duty	-	30	-	70	%

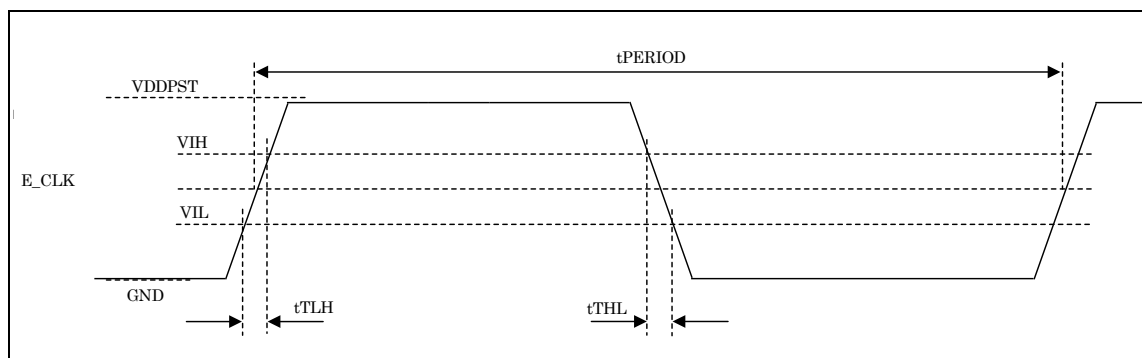


Figure 5 eMMC Interface Clock signal timing

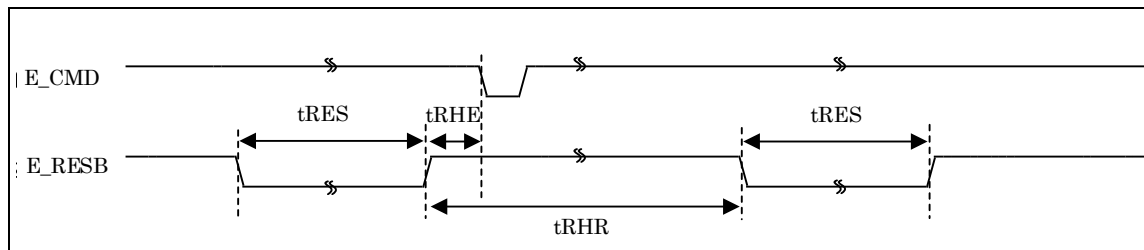
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10-1-2. Reset Timing**Table 13. eMMC Interface Reset timing**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reset Low Time	tRES	50	-	-	μs
Reset High Time (Before eMMC Access)	tRHE	100	-	-	ns
Reset High Time (Before Next Reset Low)	tRHR	300	-	-	μs

**Figure 6. eMMC Interface Reset timing**

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10-1-3. Input Timing

Table 14. eMMC Interface Device input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Command/Data Setup Time	tISU	1.40	-	-	ns
Command/Data Hold Time	tIH	0.8	-	-	ns

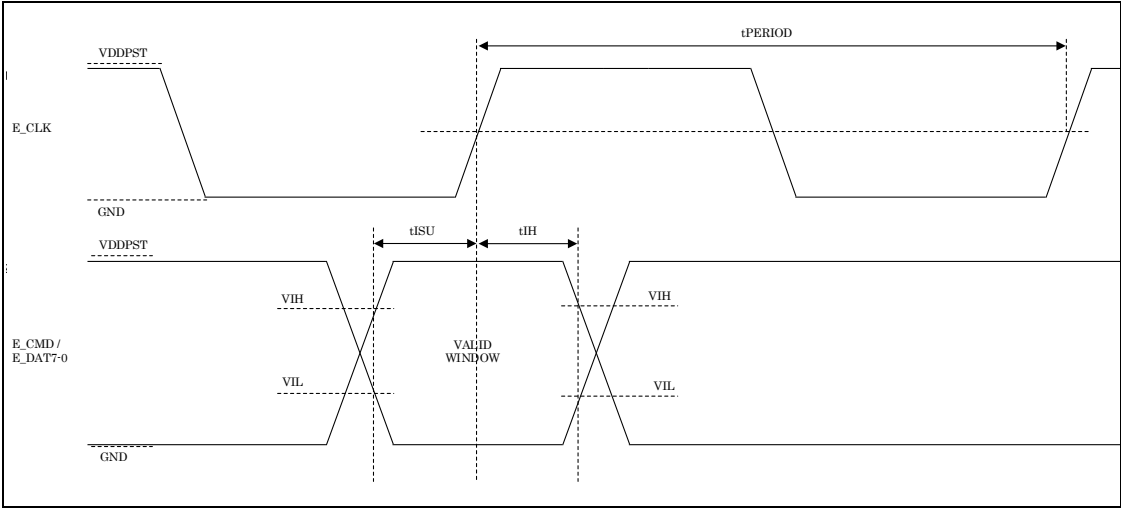


Figure 7. eMMC Interface input timing

10-1-4. Output Timing

Table 15. eMMC Interface output timing

(Load=15pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Command/Data output delay	tPH	0	-	2	UI *1
Output delay variation range	Δ TPH	-	-	1900	ps *2
Command/Data valid window	tVW	0.575	-	-	UI *1

*1 Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz

*2 Δ TPH is total allowable shift of output valid window at temperature from 0 °C to 125 °C

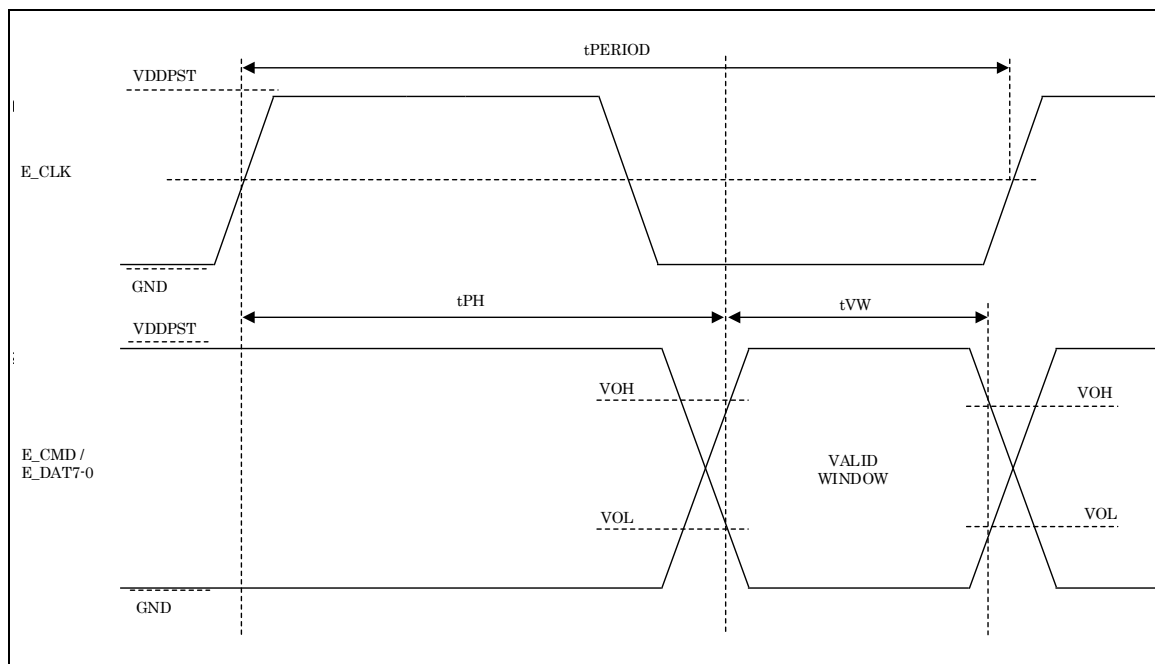


Figure 8. eMMC Interface output timing

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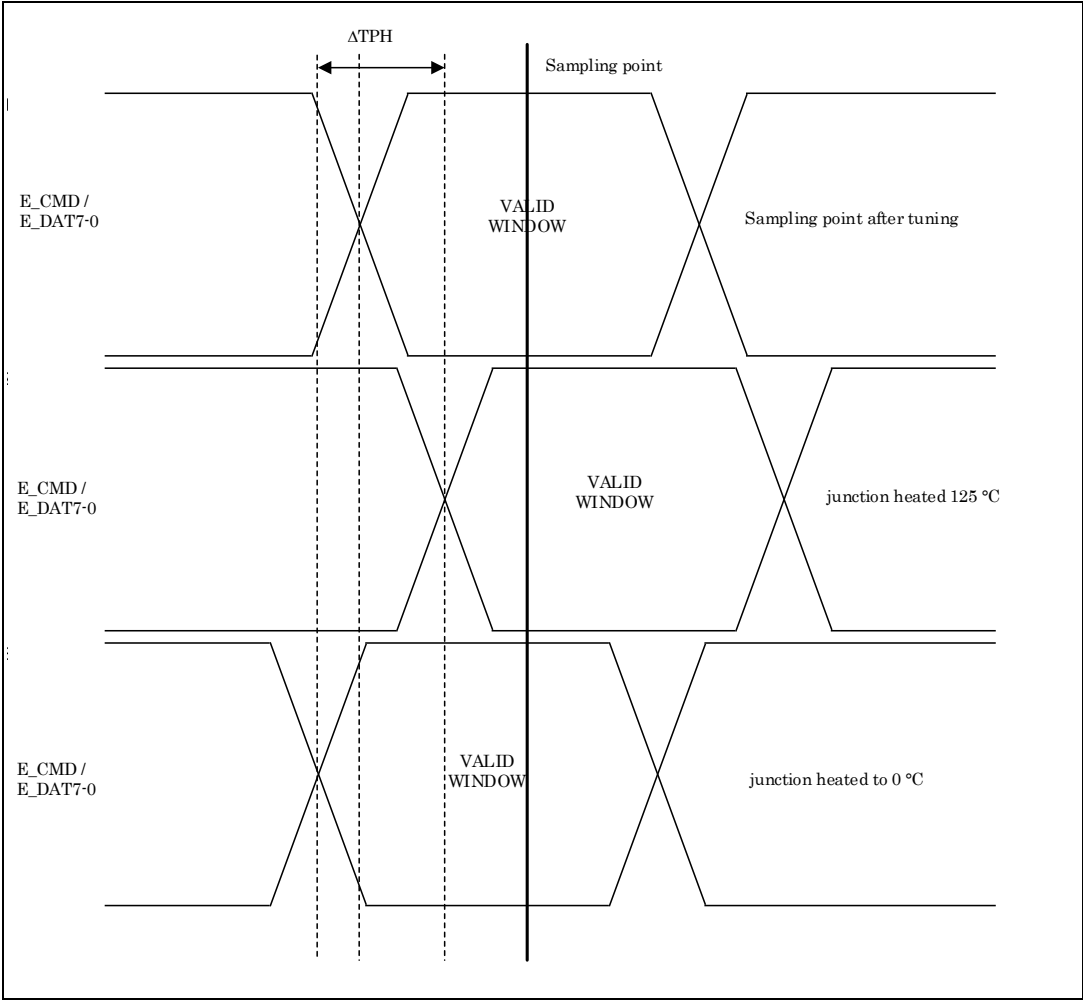


Figure 9. ΔT_{PH} consideration

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10-2. Game Memory Interface**10-2-1. 16Byte Command****Table 16. Game Memory Interface AC Characteristics (66.7MHz)**

(Load=25pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Cycle Time	tWC	14.4(T.B.D.)	15	-	ns
CLK High Pulse Width	tWH	7	7.5	-	ns
CLK Low Pulse Width	tWL	7	7.5	-	ns
CEB Low to CLK Low Time	tCS	90	-	-	ns
CLK High to CEB High Time	tCH	60	-	-	ns
CEB High Pulse Width	tCEPH	10	-	-	μs
Data Output Delay	tDLY	3	-	10.8	ns
Data Strobe Cycle Time	tSWC	14.4	-	-	ns
Data Strobe High Pulse Width	tSWH	5	-	-	ns
Data Strobe Low Pulse Width	tSWL	5	-	-	ns
Data Setup Time with Data Strobe	tSDS	4	-	-	ns
Data Hold Time with Data Strobe	tSDH	4	-	-	ns
Data Valid Time	tDV	3	-	-	ns
Data Strobe Delay	tDQSD	-	-	90	ns
Output to Hi-Z Time	tDHz	-	-	15	ns
Hi-Z to Output Time	tHZD	-	-	10.8	ns
Wait1 Cycle	tWAIT1	0	-	*2	cyc
Wait2 Cycle	tWAIT2	0	-	*2	cyc
Latency1 Cycle	tHZ1	2			cyc
Latency2 Cycle	tHZ2	1 *3			cyc
Latency3 Cycle	tHZ3	1			cyc

*1 cyc means C_CLK toggling 1 time, normally this time is tWC time.

For example, 1cyc = 15ns at 66.7MHz Typical.

*2 Wait Cycle is Configurable, Max 64M cycle.

*3 tHZ2 time is extended by Data Strobe Delay Time, for bus fight prevention.

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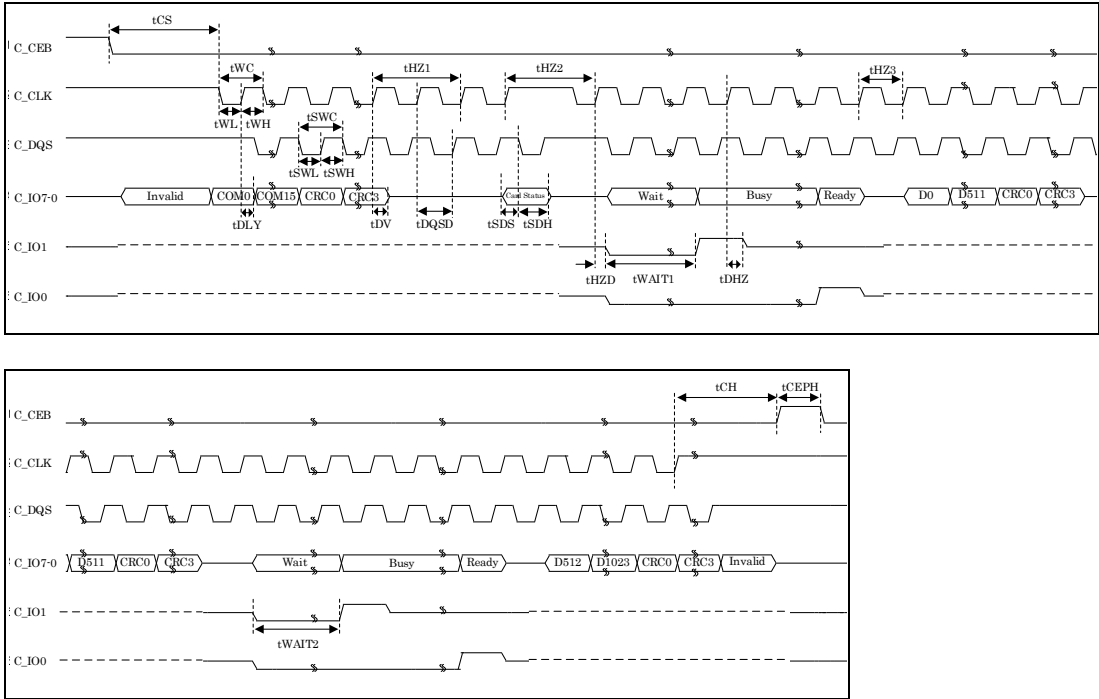


Figure 10. Game Memory Interface AC Characteristics (16Byte Command Data Read) (66.7MHz)

Table 17. Game Memory Interface AC Characteristics (50MHz)

(Load=25pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Cycle Time	tWC	19.2	20	-	ns
CLK High Pulse Width	tWH	9.5	10	-	ns
CLK Low Pulse Width	tWL	9.5	10	-	ns
CEB Low to CLK Low Time	tCS	90	-	-	ns
CLK High to CEB High Time	tCH	60	-	-	ns
CEB High Pulse Width	tCEPH	10	-	-	µs
Data Output Delay	tDLY	4	-	10.8	ns
Data Strobe Cycle Time	tSWC	19.2	-	-	ns
Data Strobe High Pulse Width	tSWH	5	-	-	ns
Data Strobe Low Pulse Width	tSWL	5	-	-	ns
Data Setup Time with Data Strobe	tSDS	5	-	-	ns
Data Hold Time with Data Strobe	tSDH	5	-	-	ns
Data Valid Time	tDV	4	-	-	ns
Data Strobe Delay	tDQSD	-	-	120	ns
Output to Hi-Z Time	tDHz	-	-	20	ns
Hi-Z to Output Time	tHZD	-	-	15.6	ns
Wait1 Cycle	tWAIT1	0	-	*2	cyc
Wait2 Cycle	tWAIT2	0	-	*2	cyc
Latency1 Cycle	tHZ1	2			cyc
Latency2 Cycle	tHZ2	1 *3			cyc
Latency3 Cycle	tHZ3	1			cyc

*1 cyc means C_CLK toggling 1 time, normally this time is tWC time.

For example, 1cyc = 20ns at 50MHz Typical.

*2 Wait Cycle is Configurable, Max 64M cycle.

*3 tHZ2 time is extended by Data Strobe Delay Time, for bus fight prevention.

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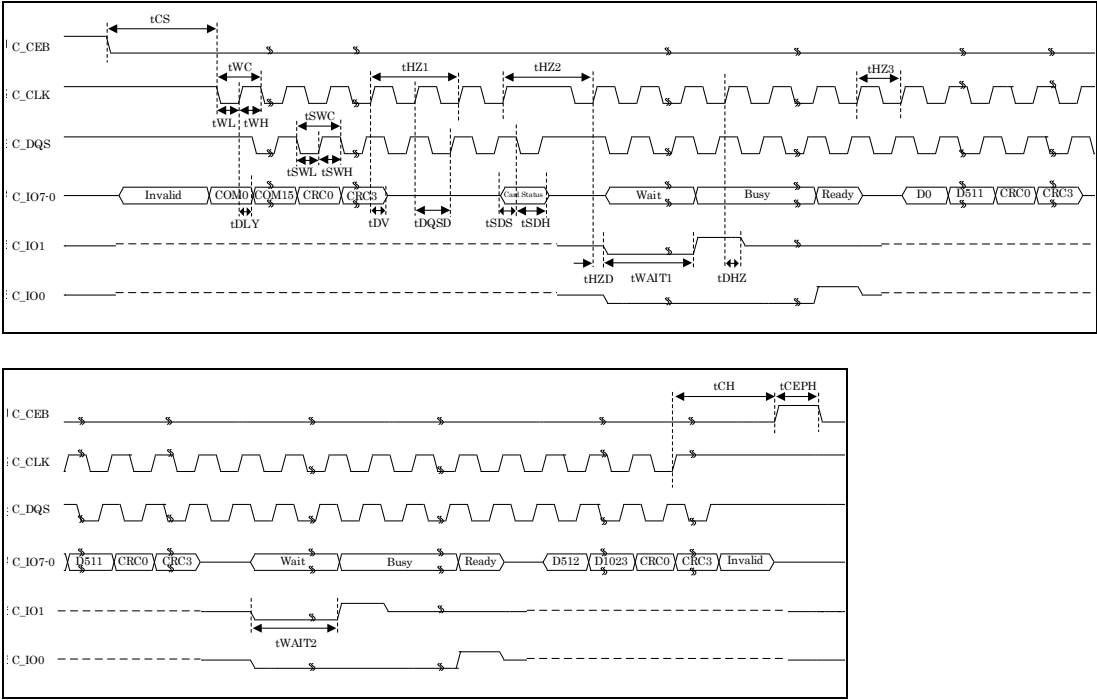


Figure 11. Game Memory Interface AC Characteristics (16Byte Command Data Read) (50MHz)

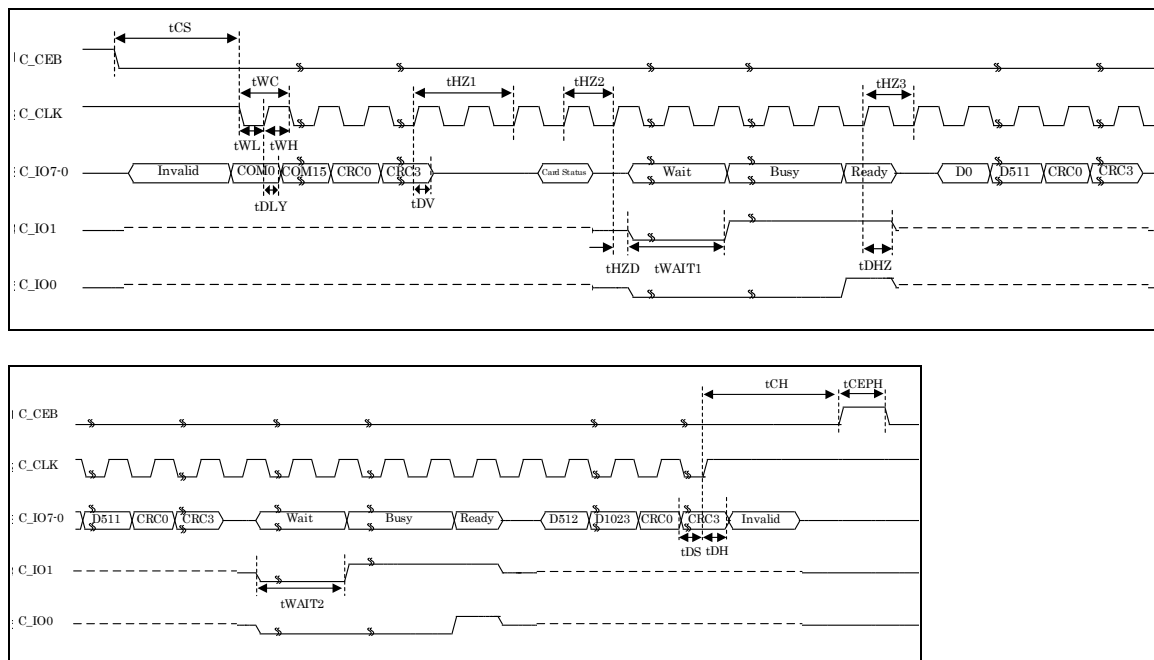
Table 18. Game Memory Interface AC Characteristics (25MHz)

(Load=25pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Cycle Time	tWC	38	40	-	ns
CLK High Pulse Width	tWH	18	20	-	ns
CLK Low Pulse Width	tWL	18	20	-	ns
CEB Low to CLK Low Time	tCS	120	-	-	ns
CLK High to CEB High Time	tCH	165	-	-	ns
CEB High Pulse Width	tCEPH	10	-	-	µs
Data Output Delay	tDLY	4	-	20	ns
Data Setup Time	tDS	11	-	-	ns
Data Hold Time	tDH	0	-	-	ns
Data Valid Time	tDV	4	-	-	ns
Output to Hi-Z Time	tDHz	-	-	26	ns
Hi-Z to Output Time	tHZD	-	-	20	ns
Wait1 Cycle	tWAIT1	0	-	*2	cyc
Wait2 Cycle	tWAIT2	0	-	*2	cyc
Latency1 Cycle	tHZ1	2			cyc
Latency2 Cycle	tHZ2	1			cyc
Latency3 Cycle	tHZ3	1			cyc

*1 cyc is tWC time. For example, 1cyc = 40ns at 25MHz Typical.

*2 Wait Cycle is Configurable, Max 64M cycle.

**Figure 12. Game Memory Interface AC Characteristics (16Byte Command Data Read) (25MHz)**

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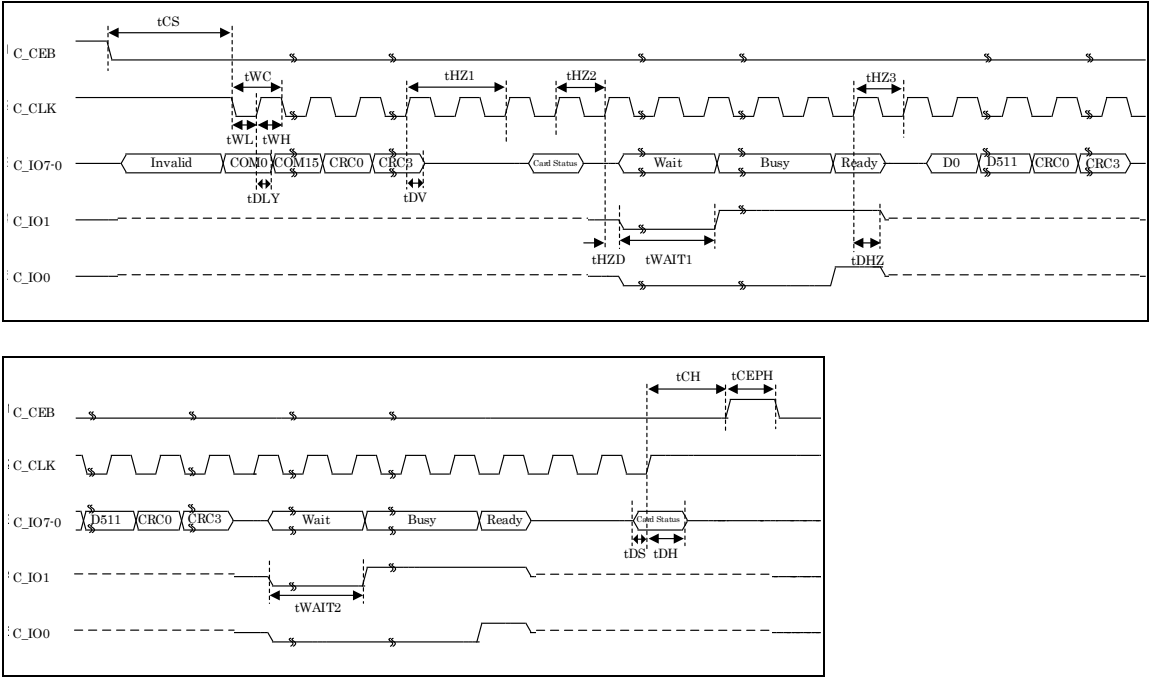


Figure 13. Game Memory Interface AC Characteristics (16Byte Command Data Write) (25MHz)

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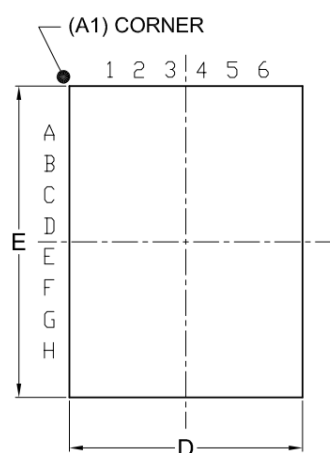
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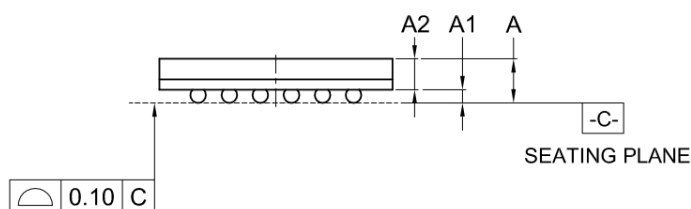
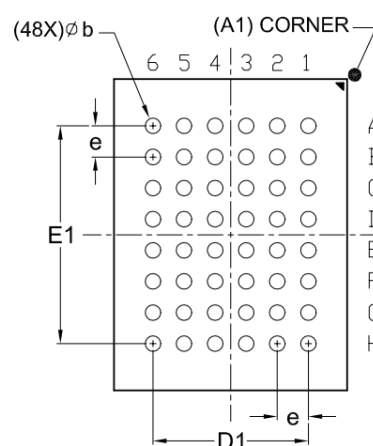
11. Package Information

Doc. Title: Package Outline for CSP 48BALL(6X8X1.3MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)

TOP VIEW



BOTTOM VIEW



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	D	D1	E	E1	e
UNIT										
mm	Min.	---	0.25	0.65	0.35	5.90		7.90		
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	5.60	0.80
	Max.	1.30	0.35	---	0.45	6.10		8.10		
Inch	Min.	---	0.010	0.026	0.014	0.232		0.311		
	Nom.	---	0.012	---	0.016	0.236	0.157	0.315	0.220	0.031
	Max.	0.051	0.014	---	0.018	0.240		0.319		

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4202	5	MO-219			