



MACRONIX
INTERNATIONAL Co., LTD.

MX23K128GL0

128G-BIT ROM TYPE GAME CARD MEMORY DATASHEET

Contents

1. FEATURES	4
2. GENERAL DESCRIPTION	4
3. PIN CONFIGURATIONS.....	5
4. PIN DESCRIPTION.....	5
5. BLOCK DIAGRAM	6
Figure 1. Block Diagram	6
6. CARD STATUS DEFINITION	7
Table 1. Card Status	7
7. ID DEFINITION	8
Table 2. RD_ID1/t1RD_ID1	8
Table 3. RD_ID2/t1RD_ID2.....	8
Table 4. RD_ID3/t1RD_ID3.....	8
8. RES DEFINITION	9
Table 5. RD_SELF_REFRESH.....	9
Table 6. RD_REFRESH_STATUS	9
9. ABSOLUTE MAXIMUM RATINGS.....	10
10.RECOMMENDED OPERATING CONDITIONS	10
11.DC CHARACTERISTICS.....	11
Table 7. DC Characteristics ($T_A = 0\sim 60^{\circ}\text{C}$, $V_{CC} = 2.8\sim 3.4\text{V}$, $V_{CCIO} = 1.62\sim 1.98\text{V}$).....	11
Figure 2. Standby Current (ISTB1)	12
Figure 3. Standby Current (ISTB2)	12
12.CAPACITANCE	13
Table 8. Capacitance ($T_A = 0\sim 60^{\circ}\text{C}$, $V_{CC} = 2.8\sim 3.4\text{V}$, $V_{CCIO} = 1.62\sim 1.98\text{V}$, $f = 1.0\text{MHz}$)	13
13.AC CHARACTERISTICS.....	13
Table 9. AC TEST CONDITION	13
Table 10. AC Characteristics (50MHz, $T_A = 0\sim 60^{\circ}\text{C}$, $V_{CC} = 2.8\sim 3.4\text{V}$, $V_{CCIO} = 1.62\sim 1.98\text{V}$).....	14
Table 11. AC Characteristics (25MHz, $T_A = 0\sim 60^{\circ}\text{C}$, $V_{CC} = 2.8\sim 3.4\text{V}$, $V_{CCIO} = 1.62\sim 1.98\text{V}$).....	15
Table 12. AC Characteristics for RESB Timing ($T_A = 0\sim 60^{\circ}\text{C}$, $V_{CC} = 2.8\sim 3.4\text{V}$, $V_{CCIO} = 1.62\sim 1.98\text{V}$)	16
Figure 4. RESB Timing Waveform (Case1)	16



Figure 5. RESB Timing Waveform (Case 2)	17
Figure 6. Command Input and Data Output Timing Waveform (Read, 50MHz)	18
Figure 7. Command Input and Data Output Timing Waveform (Read, 25MHz)	18
Figure 8. Ready/Busy Timing Waveform (Read, 50MHz)	19
Figure 9. Ready/Busy Timing Waveform (Read, 25MHz)	19
Figure 10. Standby Mode Timing Waveform.....	19
14. PACKAGE INFORMATION	20

1. FEATURES

- Voltage Supply
 - VCC : 3.1V
 - VCCIO : 1.8V
- Organization
 - 16384M x 8bit
- Read Operation
 - Page Size: 512 Byte
 - Read Cycle Time: 19.2ns (Min.)
- Current
 - Read: 190mA
 - Standby: 600uA
- Command/Address/Data Multiplexed Port
- Security Embedded
- Power On Reset Function
- Package: LGA 16L

2. GENERAL DESCRIPTION

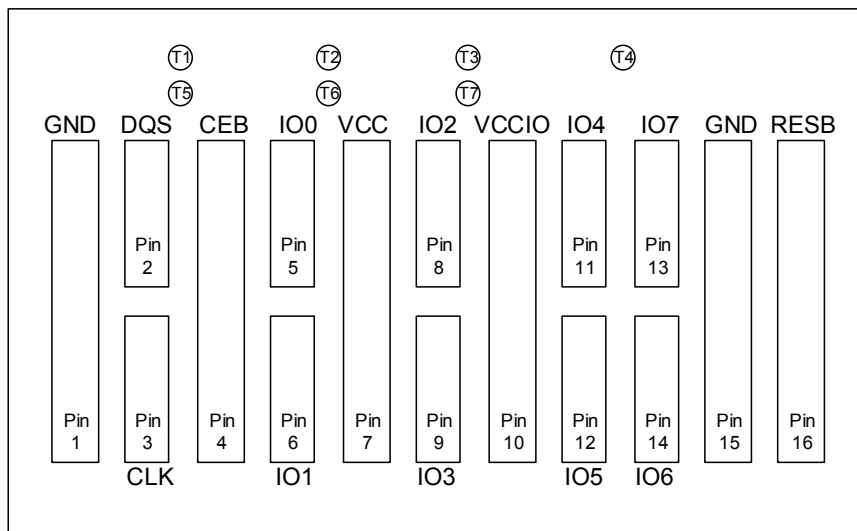
The MX23K128GL0 is a 128Gbit factory pre-programmed MLC NAND (ROM TYPE) with 3.1V and IO 1.8V.

It is a bidirectional device, which utilizes the 8 bit multiplexed I/O bus for command, address, and data inputs/outputs.

Simple design structure makes the cost of the device competitive over the other types of code-storage memory IC.

3. PIN CONFIGURATIONS

LGA 16L



4. PIN DESCRIPTION

SYMBOL	PIN#	TYPE	DESCRIPTION
GND	1, 15	I	Ground
DQS	2	O	Feedback Clock of CLK (Data Strobe Signal)
CLK	3	I	Clock Signal
CEB	4	I	Chip Enable Signal 0 : Enable 1 : Disable
IO0	5	I/O	Command/Address/Data/Ready/Busy Multiplexed I/O Port
IO1	6	I/O	Command/Address/Data/Wait Multiplexed I/O Port
IO2~IO7	8, 9, 11~14	I/O	Command/Address/Data Multiplexed I/O Port
VCC	7	I	Power (3.1V, for Internal Core)
VCCIO	10	I	Power (1.8V, for I/O)
RESB	16	I	Reset Signal 0 : Device Reset
T1~T7	-	-	Test Pins, no connection

5. BLOCK DIAGRAM

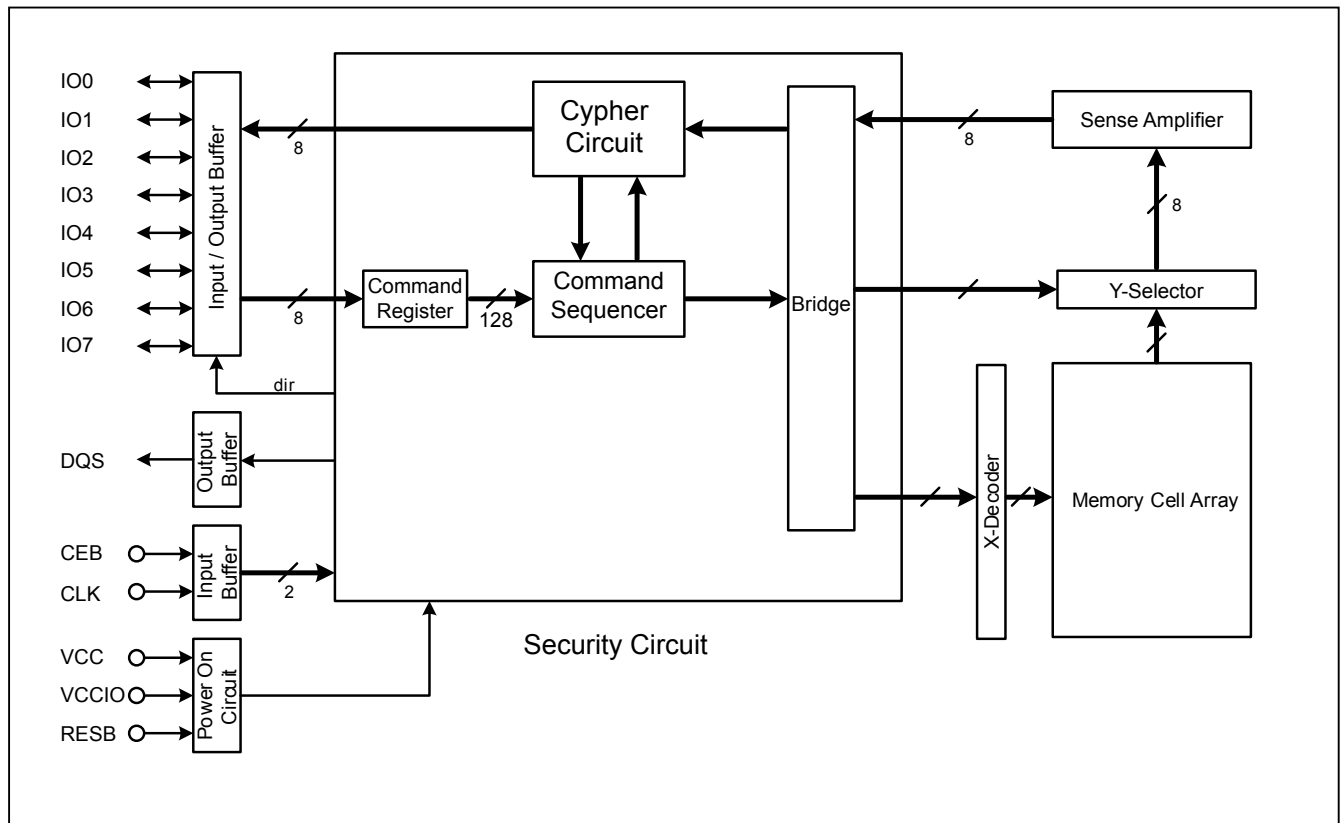


Figure 1. Block Diagram

6. CARD STATUS DEFINITION**Table 1. Card Status**

	DESCRIPTION
bit0	CRC Error Flag 0: No Error 1: Error
bit1	0
bit2	Fatal Error Flag 0: No Error 1: Error
bit3	Refresh Request Flag 0: Not Refresh Request 1: Refresh Request
bit4-7	0h

7. ID DEFINITION

Table 2. RD_ID1/t1RD_ID1

ID1	VALUES	DESCRIPTION
ID1_0	C2h	Maker Code
ID1_1	E1h	Memory Size
ID1_2	02h	Option1
ID1_3	21h (Note1)	Memory Type

Note1: bit7 Reserved = 0
 bit6 Reserved = 0
 bit5 0: tRB_5 ≤ 100us
 1: tRB_5 > 100us
 bit4 Reserved = 0
 bit3 0: ROM Type
 1: R/W Type
 bit2 Reserved = 0
 bit[1:0] 00: Reserved
 01: T1
 10: T2
 11: Reserved

Note2: tRB_5 means tRB_N5 and tRB_S5.

Table 3. RD_ID2/t1RD_ID2

ID2	VALUES	DESCRIPTION
ID2_0	02h	Option1
ID2_1	00h	Option2
ID2_2	00h	Option3
ID2_3	00h	Option4

Table 4. RD_ID3/t1RD_ID3

ID3	VALUES	DESCRIPTION
ID3_0	00h	Option1
ID3_1	00h	Option2
ID3_2	00h	Option3
ID3_3	00h	Option4

8. RES DEFINITION**Table 5. RD_SELF_REFRESH**

RES	VALUES	DESCRIPTION
RES0	00h (Note1)	Self Refresh Status
	01h (Note2)	
RES1	00h	Response1
RES2	00h	Response2
RES3	00h	Response3

Note 1: Unnecessary

Note 2: Self Refresh Start

Table 6. RD_REFRESH_STATUS

RES	VALUES	DESCRIPTION
RES0	00h (Note1)	Self Refresh Status
	01h (Note2)	
	03h (Note3)	
	FFh (Note4)	
RES1	00h ~ 0Fh (Note5)	Self Refresh Sum Total
RES2	00h (Note6)	Self Refresh Error
	01h (Note7)	
RES3	00h	Response1

Note 1: Finish (No Error)

Note 2: Executing

Note 3: Finish (Error)

Note 4: Non-Execute

Note 5: Success Count (RES1 ≥ 0Fh is 0Fh)

Note 6: No Error

Note 7: Error

9. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS
Power Supply Voltage1	V_{CC}	-0.5V to 4.6V
Power Supply Voltage2	V_{CCIO}	-0.5V to 2.5V
Input Voltage	V_{IN}	-0.3V to V_{CCIO} +0.3V (Note1)
Output Voltage	V_{OUT}	-0.3V to V_{CCIO} +0.3V (Note1)
Ambient Operating Temperature	T_{OPR}	0°C to 60°C
Storage Temperature	T_{STG}	-25°C to 85°C

Note1:

Minimum DC voltage on input or I/O pins is -0.3V. During voltage transitions, inputs may undershoot GND to -1.3V for periods of up to 20ns.

Maximum DC voltage on input or I/O pins is V_{CCIO} +0.3V. During voltage transitions, inputs may overshoot V_{CCIO} to V_{CCIO} +2.0V for periods of up to 20ns.

10. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature	T_A	0	25	60	°C
Power Supply Voltage	V_{CC}	2.8	3.1	3.4	V
IO Power Supply Voltage	V_{CCIO}	1.62	1.8	1.98	V

11. DC CHARACTERISTICS

Table 7. DC Characteristics ($T_A = 0 \sim 60^\circ\text{C}$, $V_{CC} = 2.8 \sim 3.4\text{V}$, $V_{CCIO} = 1.62 \sim 1.98\text{V}$)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	MAX.	UNIT
Input High Voltage	V _{IH}	-		0.75 * V _{CCIO}	V _{CCIO} + 0.3	V
Input Low Voltage	V _{IL}	-		-0.3	0.3 * V _{CCIO}	V
Schmitt Trigger Input (L to H) (CLK, CEB)	V _{t+}	-		-	0.7 * V _{CCIO}	V
Schmitt Trigger Input (H to L) (CLK, CEB)	V _{t-}	-		0.3 * V _{CCIO}	-	V
Schmitt Trigger Hysteresis Voltage (CLK, CEB)	(delta)V _t	-		0.15	-	V
Output High Voltage	V _{OH}	I _{OH} = -400uA		0.85 * V _{CCIO}	-	V
Output Low Voltage	V _{OL}	I _{OL} = 1.6mA		-	0.1 * V _{CCIO}	V
Operating Current1	I _{CC1-1}	tWC = 20ns		-	190	mA
	I _{CC1-2}	tWC = 40ns		-	140	mA
Operating Current2	I _{CCIO2-1}	tWC = 20ns		-	30	mA
	I _{CCIO2-2}	tWC = 40ns		-	20	mA
Standby Current1	I _{CC_STB1}	CEB = V _{CCIO} - 0.2V, IO=V _{CCIO} - 0.2V or 0.2V, CLK = V _{CCIO} - 0.2V	T _A =25°C	-	600	uA
			T _A =60°C	-	1000	uA
	I _{CCIO_STB1}	CEB = V _{CCIO} - 0.2V, IO=V _{CCIO} - 0.2V or 0.2V, CLK = V _{CCIO} - 0.2V	T _A =25°C	-	100	uA
			T _A =60°C	-	200	uA
Standby Current2	I _{CC_STB2}	CEB = V _{CCIO} - 0.2V, IO=V _{CCIO} - 0.2V or 0.2V, tWC = 20ns (Duty 50%)	T _A =25°C	-	600	uA
			T _A =60°C	-	1000	uA
	I _{CCIO_STB2}	CEB = V _{CCIO} - 0.2V, IO=V _{CCIO} - 0.2V or 0.2V, tWC = 20ns (Duty 50%)	T _A =25°C	-	100	uA
			T _A =60°C	-	200	uA
Input Leakage Current	I _{LI}	V _{IN} = 0 to V _{CC} (max)		-	±10	uA
Output Leakage Current	I _{LO}	V _{OUT} = 0 to V _{CC} (max)		-	±10	uA

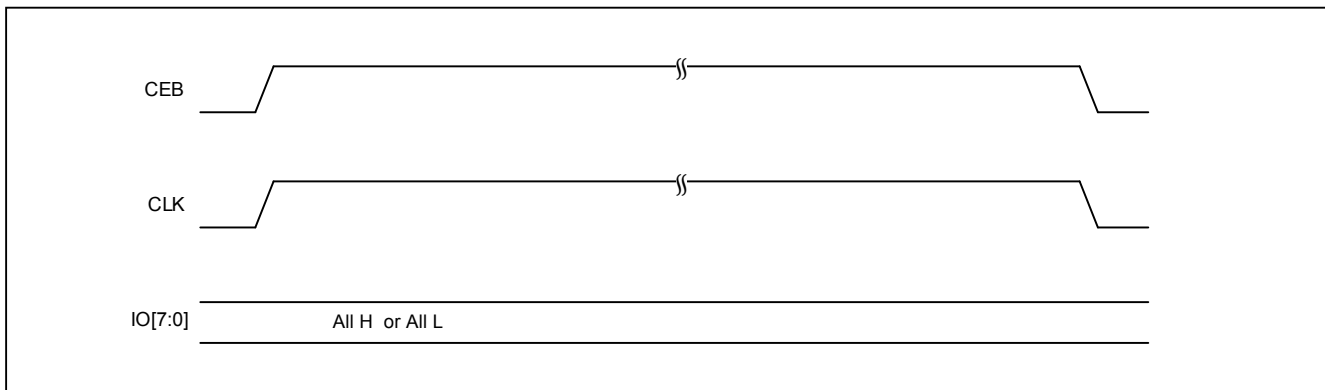


Figure 2. Standby Current (ISTB1)

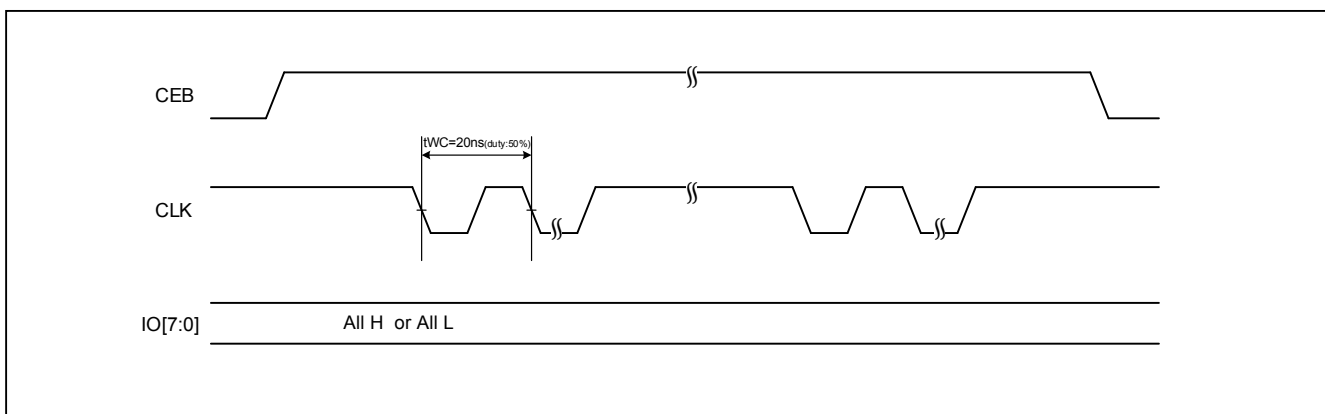


Figure 3. Standby Current (ISTB2)

12. CAPACITANCE

Table 8. Capacitance ($T_A = 0\sim 60^\circ\text{C}$, $V_{CC} = 2.8\sim 3.4\text{V}$, $V_{CCIO} = 1.62\sim 1.98\text{V}$, $f = 1.0\text{MHz}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Output Capacitance	C_{OUT}	$V_{OUT} = 0\text{V}$	-	15	pF
Input Capacitance	C_{IN}	$V_{IN} = 0\text{V}$	-	15	pF

13. AC CHARACTERISTICS

Table 9. AC TEST CONDITION

PARAMETER	TEST CONDITIONS
Input Pulse Level	$V_{CCIO} * 0.1$ to $V_{CCIO} * 0.9$
Input Rise and Fall Times	3ns
Input Timing Levels (CLK)	$V_{CCIO} * 0.5$
Input Timing Levels (CEB, IO, RESB)	$V_{CCIO} * 0.3$ to $V_{CCIO} * 0.7$
Output Timing Levels	0.45V to $V_{CCIO} - 0.45\text{V}$
Output Load	30pF

Note 1: $V_{CCIO} = 1.62\text{V}\sim 1.98\text{V}$

Table 10. AC Characteristics (50MHz, T_A = 0~60°C, V_{CC} = 2.8~3.4V, V_{CCIO} = 1.62~1.98V)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
CLK Cycle Time		tWC	19.2	20	-	ns
CLK High Pulse Width		tWH	9	10	-	ns
CLK Low Pulse Width		tWL	9	10	-	ns
CEB Setup Time		tCS	90	-	-	ns
CEB Hold Time		tCH	60	-	-	ns
CEB High Pulse Width		tCEPH	300	-	-	ns
Data Setup Time		tDS	3	-	-	ns
Data Hold Time		tDH	4	-	-	ns
Data Valid Time		tDV	0	-	-	ns
CLK Access Time (Note4)		tREA	0	-	40	ns
DQS Delay Time		tDQSD	0	-	40	ns
DQS Cycle Time		tSWC	19.2	-	-	ns
DQS Hith Pulse Width		tSWH	5	-	-	ns
DQS Low Pulse Width		tSWL	5	-	-	ns
DQS Data Setup Time		tSDS	5	-	-	ns
DQS Data Hold Time		tSDH	5	-	-	ns
Ready/Busy1	RD_ID1	tRB_N1	2			cycle
	RD_ID2	tRB_N2	2			cycle
	RD_ID3	tRB_N3	2			cycle
	CHG_INIT	tRB_N4	2			cycle
	RD_PAGE	tRB_N5	-	-	30	ms
	RD_SELF_REFRESH (Note3)	tRB_N6	-	-	300	us
	RD_REFRESH_STATUS	tRB_N7	6			cycle
	iRD_INIT	tRB_I1	-	-	30	ms
	iSET_INIT1	tRB_I2	314			cycle
	iSET_GEN_RAND	tRB_I3	-	-	400	us
	iSET_INIT2	tRB_I4	314			cycle
	t1RD_ID1	tRB_S1	18	-	24	cycle
	t1RD_ID2	tRB_S2	18	-	24	cycle
	t1RD_ID3	tRB_S3	18	-	24	cycle
	t1RD_UID	tRB_S4	-	-	400	us
	t1RD_PAGE	tRB_S5	-	-	10	ms
	t1RD_REFRESH	tRB_S6	26cycle	-	600	ms
	t1RD_SET_KEY	tRB_S7	314			cycle
Ready/Busy2	RD_PAGE	tRB2_N1	2cycle	-	1.5	ms
	t1RD_PAGE	tRB2_S1	2cycle	-	1.5	ms
CEB High to Output Hi-Z Time (Note1)		tCHZ	-	-	30	ns
Output to Hi-Z Time (Note1)		tSDHZ	-	-	15	ns
Latency1		tHZ1	2			cycle
Latency2		tHZ2	1			cycle
Latency3		tHZ3	1			cycle
Active to Standby Time (Note1)		tAST	-	-	15	us

Note1: This spec is guaranteed with design specification, not tested.

Note2: tRB_* and tRB2_* are based on Wait=0cycle.

Note3: It needs to issue RD_PAGE before RD_SELF_REFRESH at least once.

Note4: Data always starts to output after CLK rising edge.

Table 11. AC Characteristics (25MHz, T_A = 0~60°C, V_{CC} = 2.8~3.4V, V_{CCIO} = 1.62~1.98V)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
CLK Cycle Time		tWC	38	40	-	ns
CLK High Pulse Width		tWH	18	20	-	ns
CLK Low Pulse Width		tWL	18	20	-	ns
CEB Setup Time		tCS	120	-	-	ns
CEB Hold Time		tCH	165	-	-	ns
CEB High Pulse Width		tCEPH	300	-	-	ns
Data Setup Time		tDS	15	-	-	ns
Data Hold Time		tDH	4	-	-	ns
Data Valid Time		tDV	0	-	-	ns
CLK Access Time (Note4)		tREA	0	-	27	ns
Ready/Busy1	RD_ID1	tRB_N1	2			cycle
	RD_ID2	tRB_N2	2			cycle
	RD_ID3	tRB_N3	2			cycle
	CHG_INIT	tRB_N4	2			cycle
	RD_PAGE	tRB_N5	-	-	30	ms
	RD_SELF_REFRESH (Note3)	tRB_N6	-	-	300	us
	RD_REFRESH_STATUS	tRB_N7	6			cycle
	iRD_INIT	tRB_I1	-	-	30	ms
	iSET_INIT1	tRB_I2	314			cycle
	iSET_GEN_RAND	tRB_I3	-	-	400	us
	iSET_INIT2	tRB_I4	314			cycle
	t1RD_ID1	tRB_S1	18	-	24	cycle
	t1RD_ID2	tRB_S2	18	-	24	cycle
	t1RD_ID3	tRB_S3	18	-	24	cycle
	t1RD_UID	tRB_S4	-	-	400	us
	t1RD_PAGE	tRB_S5	-	-	10	ms
	t1RD_REFRESH	tRB_S6	26cycle	-	600	ms
	t1RD_SET_KEY	tRB_S7	314			cycle
Ready/Busy2	RD_PAGE	tRB2_N1	2cycle	-	1.5	ms
	t1RD_PAGE	tRB2_S1	2cycle	-	1.5	ms
CEB High to Output Hi-Z Time (Note1)		tCHZ	-	-	30	ns
Output to Hi-Z Time (Note1)		tDHZ	-	-	38	ns
Latency1		tHZ1	2			cycle
Latency2		tHZ2	1			cycle
Latency3		tHZ3	1			cycle
Active to Standby Time (Note1)		tAST	-	-	15	us

Note1: This spec is guaranteed with design specification, not tested.

Note2: tRB_* and tRB2_* are based on Wait=0cycle.

Note3: It needs to issue RD_PAGE before RD_SELF_REFRESH at least once.

Note4: Data always starts to output after CLK rising edge.

Table 12. AC Characteristics for RESB Timing ($T_A = 0\sim 60^\circ\text{C}$, $V_{CC} = 2.8\sim 3.4\text{V}$, $V_{CCIO} = 1.62\sim 1.98\text{V}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
RESB Non-Active Time	tRNA	9	-	-	us
RESB Low Time 1	tRES1	100	-	-	us
RESB High Time 1	tRH1	250	-	-	ms
RESB Setup Time	tRS	100	-	-	ns
RESB Low Time 2	tRES2	1	-	-	us
RESB High Time 2	tRH2	250	-	-	ms

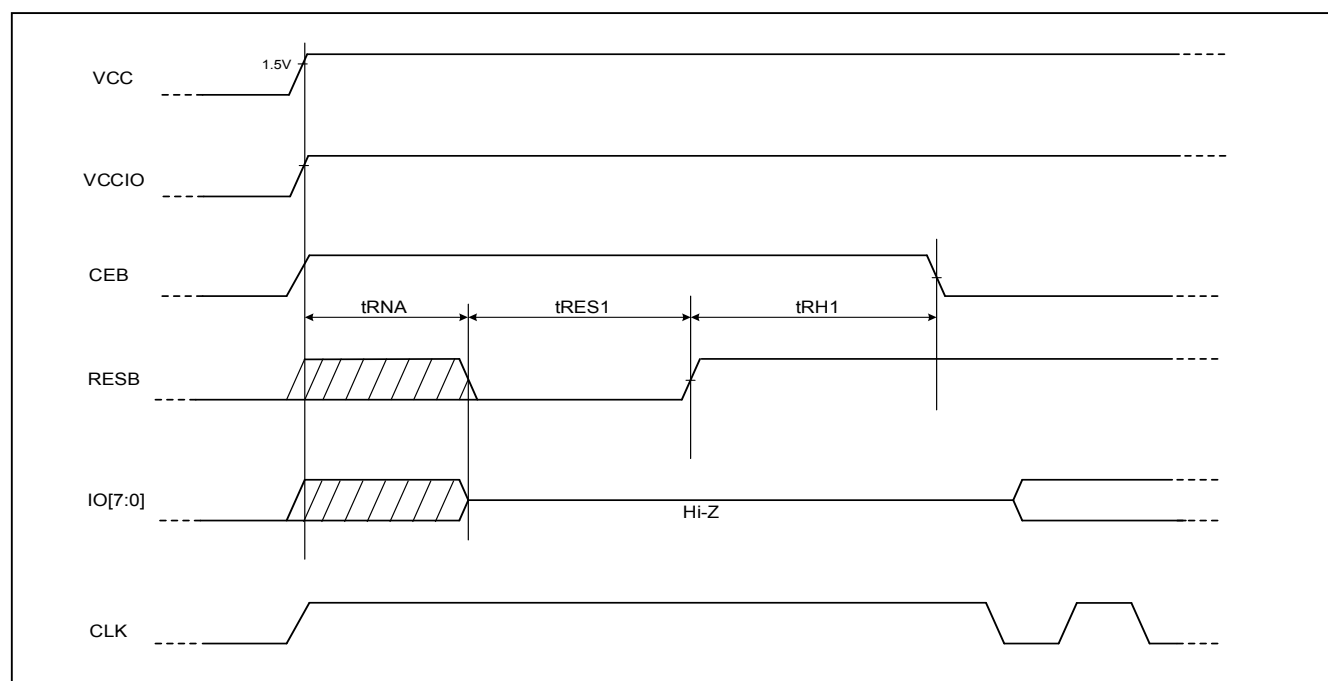
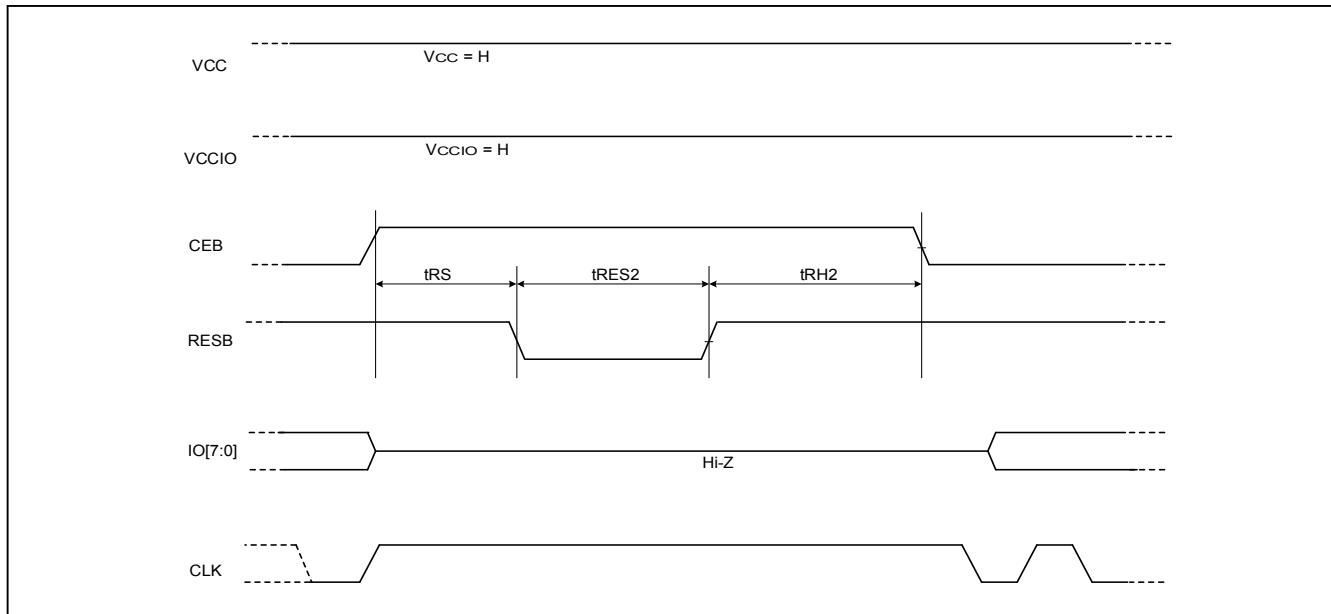


Figure 4. RESB Timing Waveform (Case1)

Note 1: During "RESB=L", IO7~IO0 is Hi-Z.

Note 2: RESB from low to high will triggered POR function during tRH1.

**Figure 5. RESB Timing Waveform (Case 2)**

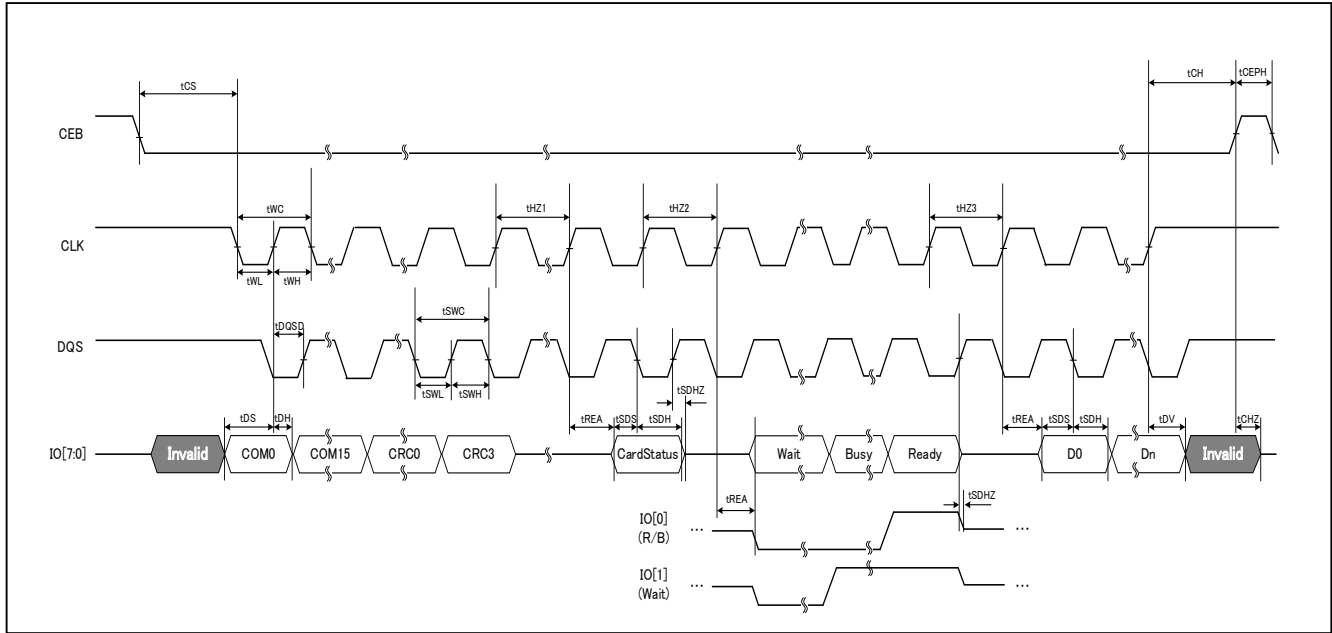


Figure 6. Command Input and Data Output Timing Waveform (Read, 50MHz)

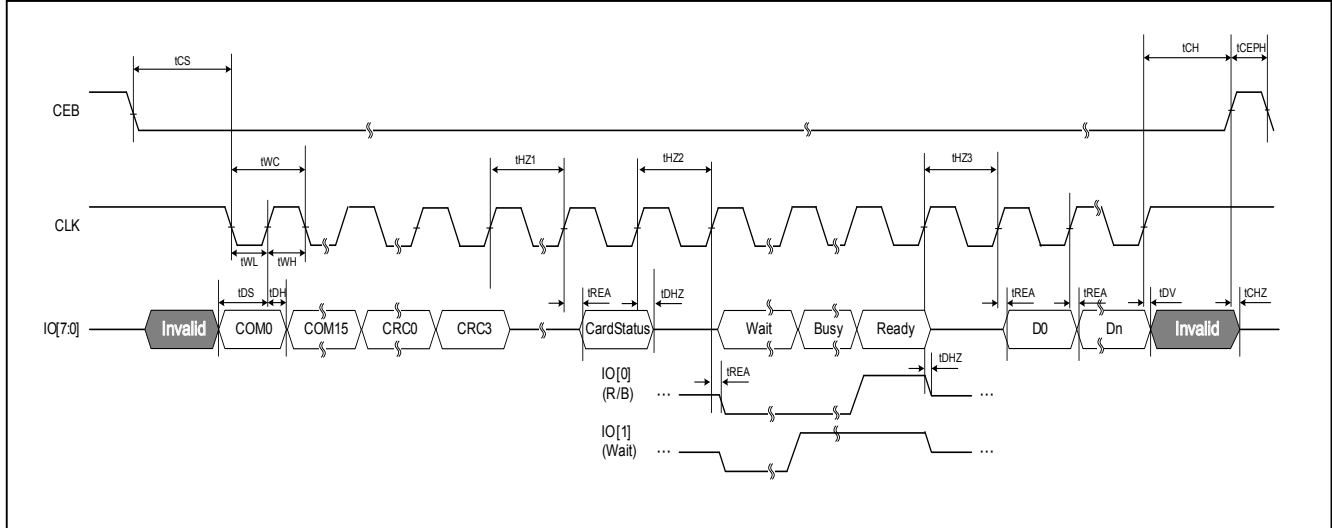


Figure 7. Command Input and Data Output Timing Waveform (Read, 25MHz)

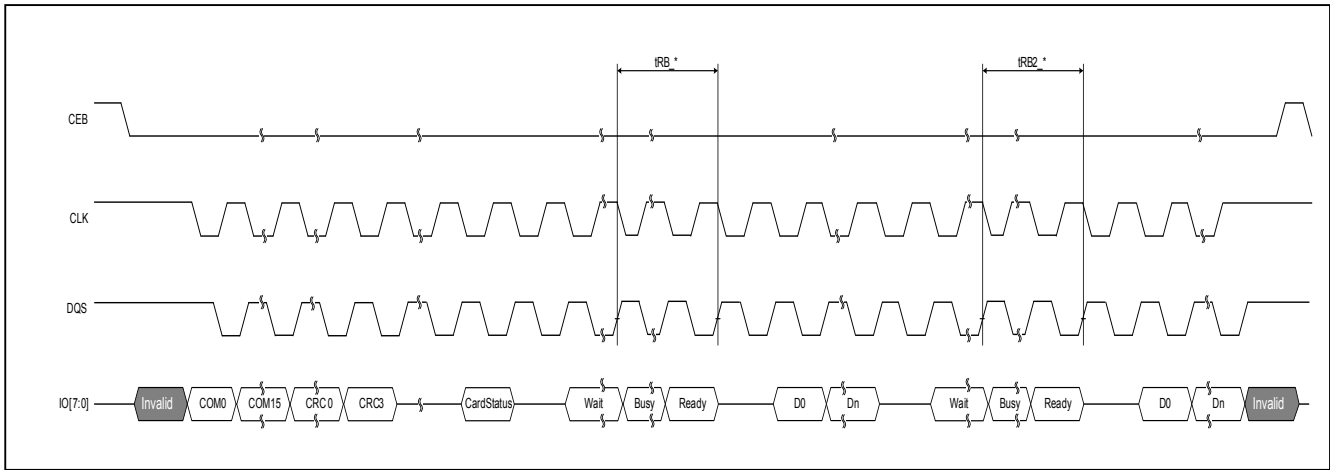


Figure 8. Ready/Busy Timing Waveform (Read, 50MHz)

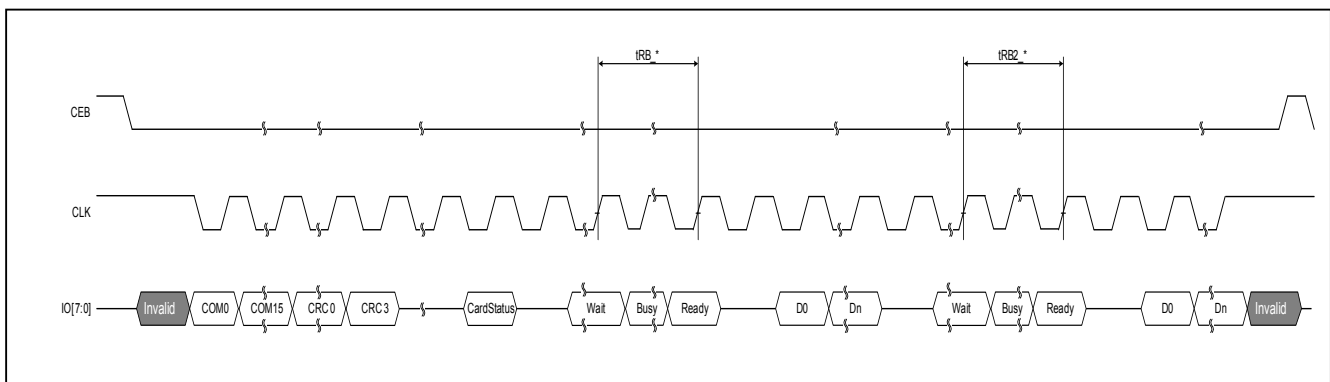


Figure 9. Ready/Busy Timing Waveform (Read, 25MHz)

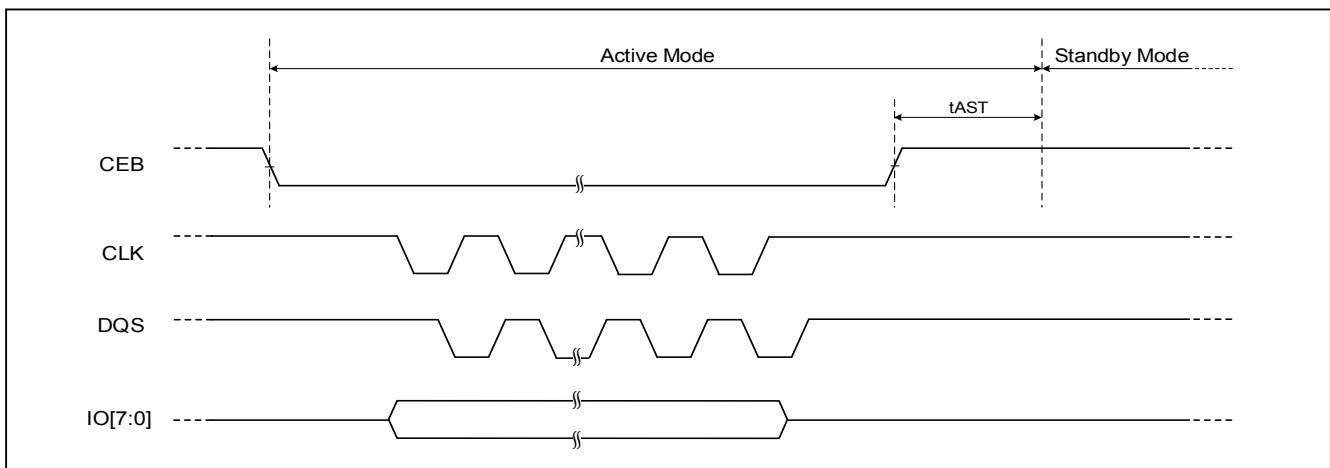
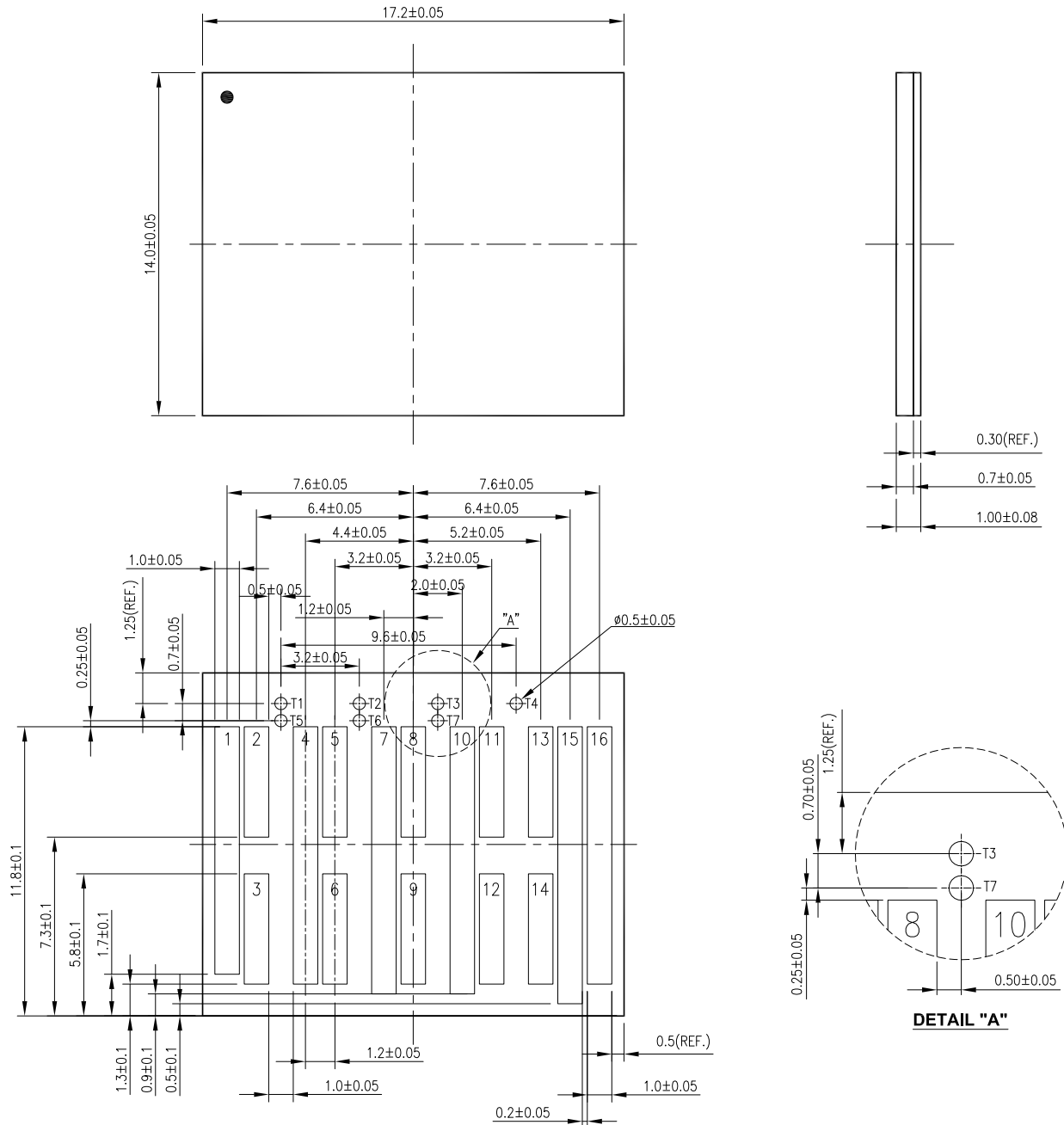


Figure 10. Standby Mode Timing Waveform

14. PACKAGE INFORMATION

Title: Package Outline for LGA 16L (17.2x14.0x1.0MM)



Dimensions Unit: mm

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-3202	0				



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MX23K128GL0

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