



MACRONIX  
INTERNATIONAL Co., LTD.

**MX23J16GL0**

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# **16G-BIT ROM TYPE GAME CARD MEMORY DATASHEET**

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### 1. FEATURES

- Voltage Supply
  - VCC : 3.1V
  - VCCIO : 1.8V
- Organization
  - 2048M x 8bit
- Read Operation
  - Page Size: 512 Byte
  - Read Cycle Time: 38ns (Min.)
- Current
  - Read: 115mA
  - Standby: 300uA
- Command/Address/Data Multiplexed Port
- Security Embedded
- Power On Reset Function
- Package: TSOP(I) 48L

### 2. GENERAL DESCRIPTION

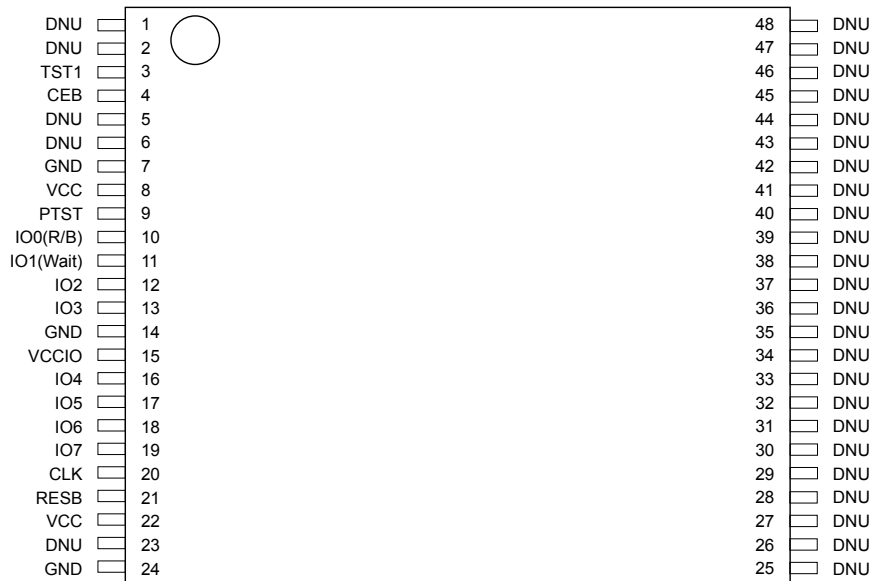
The MX23J16GL0 is a 16Gbit factory pre-programmed XtraROM with 3.1V and IO 1.8V.

It is a bidirectional device, which utilizes the 8 bit multiplexed I/O bus for command, address, and data inputs/outputs.

Simple design structure makes the cost of the device competitive over the other types of code-storage memory IC.

### 3. PIN CONFIGURATIONS

#### 48 TSOP(I)



### 4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTION
CEB	I	Chip Enable Signal 0 : Enable 1 : Disable
IO0	I/O	Command/Address/Data/ReadyBusy Multiplexed I/O Port
IO1	I/O	Command/Address/Data/Wait Multiplexed I/O Port
IO2~IO7	I/O	Command/Address/Data Multiplexed I/O Port
CLK	I	Clock Signal
RESB	I	Reset Signal 0 : Device Reset
TST1	I	Test Pin (Note 1)
PTST	I	Test Pin (Note 1)
VCC	I	Power (3.1V, for Internal Core)
VCCIO	I	Power (1.8V, for I/O)
GND	I	Ground
DNU	-	Non Connection (Note 1)

Note 1: TST1, PTST and DNU pins can be connected to GND, VCC or Open.

## 5. BLOCK DIAGRAM

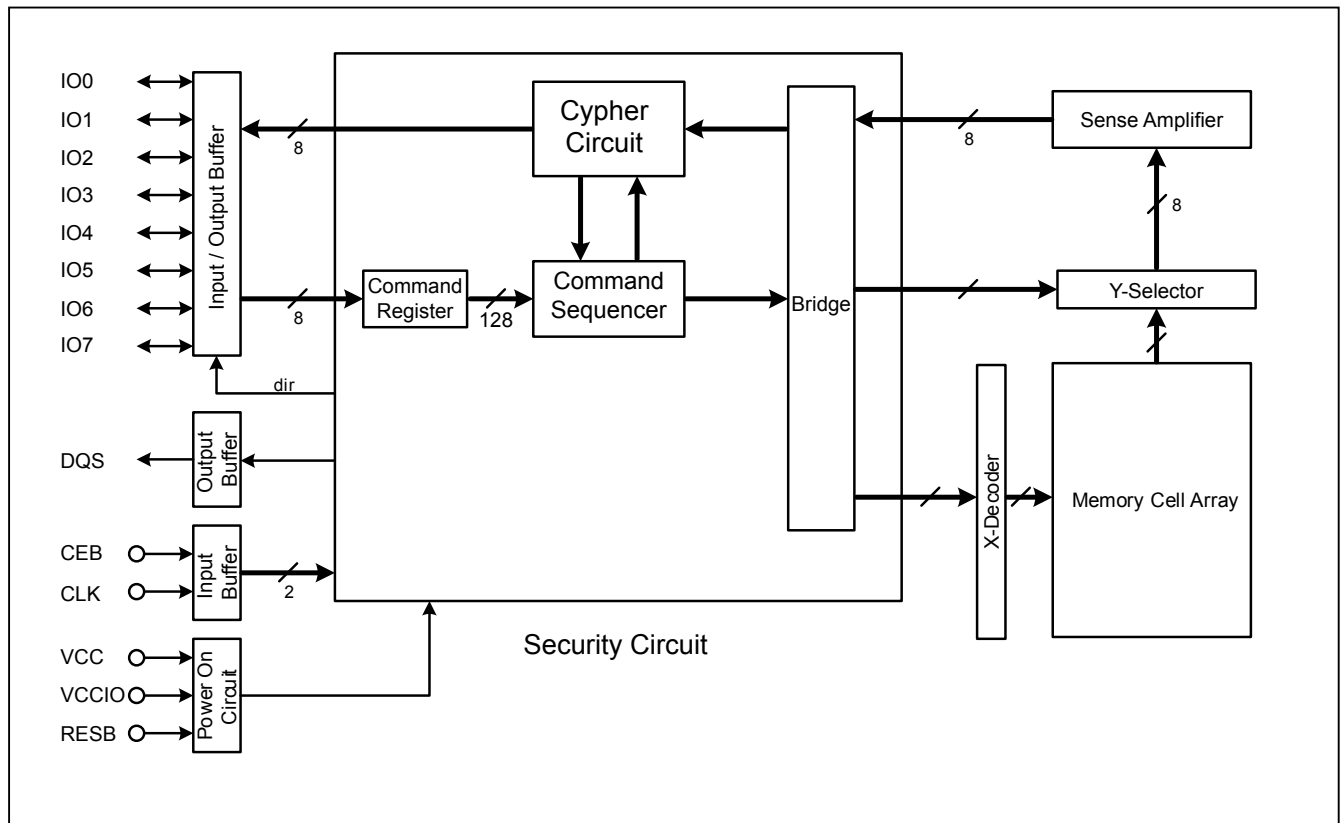


Figure 1. Block Diagram

## 6. CARD STATUS DEFINITION

Table 1. Card Status

	DESCRIPTION
bit0	CRC Error Flag 0: No Error 1: Error
bit1	0
bit2	Fatal Error Flag 0: No Error 1: Error
bit3	0
bit4-7	0h

## 7. ID DEFINITION

**Table 2. RD\_ID1/t1RD\_ID1**

ID1	VALUES	DESCRIPTION
ID1_0	C2h	Maker Code
ID1_1	F8h	Memory Size
ID1_2	00h	Option1
ID1_3	01h (Note1)	Memory Type

Note1: bit7      Reserved = 0  
bit6      Reserved = 0  
bit5      0: tRB\_5 ≤ 100us  
            1: tRB\_5 > 100us  
bit4      Reserved = 0  
bit3      0: ROM Type  
            1: R/W Type  
bit2      Reserved = 0  
bit[1:0]   00: Reserved  
            01: T1  
            10: T2  
            11: Reserved

Note2: tRB\_5 means tRB\_N5 and tRB\_S5.

**Table 3. RD\_ID2/t1RD\_ID2**

ID2	VALUES	DESCRIPTION
ID2_0	02h	Option1
ID2_1	00h	Option2
ID2_2	00h	Option3
ID2_3	00h	Option4

**Table 4. RD\_ID3/t1RD\_ID3**

ID3	VALUES	DESCRIPTION
ID3_0	00h	Option1
ID3_1	00h	Option2
ID3_2	00h	Option3
ID3_3	00h	Option4



**8. RES DEFINITION****Table 5. RD\_SELF\_REFRESH**

RES	VALUES	DESCRIPTION
RES0	00h	Response1
RES1	00h	Response2
RES2	00h	Response3
RES3	00h	Response4

**Table 6. RD\_REFRESH\_STATUS**

RES	VALUES	DESCRIPTION
RES0	FFh	Response1
RES1	00h	Response2
RES2	00h	Response3
RES3	00h	Response4

**9. ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATINGS
Power Supply Voltage1	$V_{CC}$	-0.5V to 4.6V
Power Supply Voltage2	$V_{CCIO}$	-0.5V to 2.5V
Input Voltage	$V_{IN}$	-0.3V to $V_{CCIO}$ +0.3V (Note1)
Output Voltage	$V_{OUT}$	-0.3V to $V_{CCIO}$ +0.3V (Note1)
Ambient Operating Temperature	$T_{OPR}$	0°C to 60°C
Storage Temperature	$T_{STG}$	-25°C to 85°C

Note1:

Minimum DC voltage on input or I/O pins is -0.3V. During voltage transitions, inputs may undershoot GND to -1.3V for periods of up to 20ns.

Maximum DC voltage on input or I/O pins is  $V_{CCIO}$  +0.3V. During voltage transitions, inputs may overshoot  $V_{CCIO}$  to  $V_{CCIO}$  +2.0V for periods of up to 20ns.

**10. RECOMMENDED OPERATING CONDITIONS**

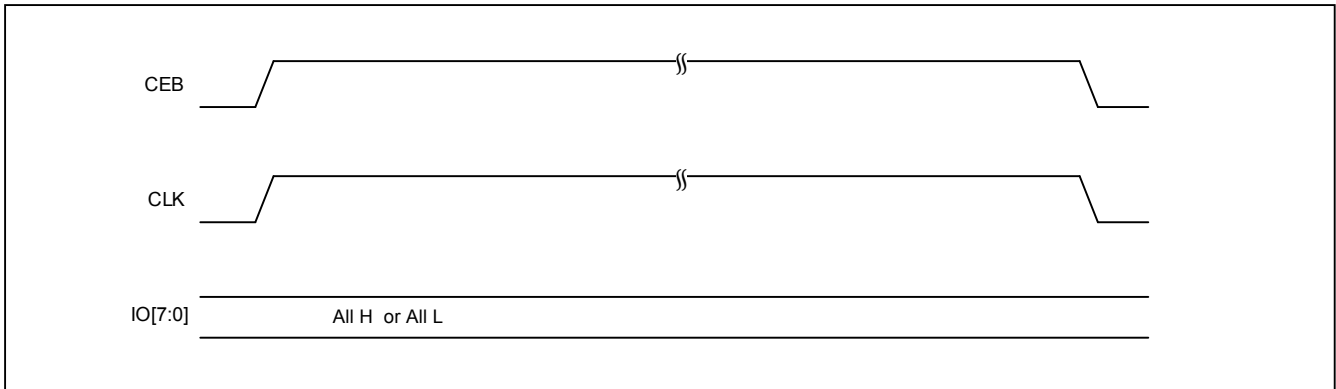
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature	$T_A$	0	25	60	°C
Power Supply Voltage	$V_{CC}$	2.8	3.1	3.4	V
IO Power Supply Voltage	$V_{CCIO}$	1.62	1.8	1.98	V

## 11. DC CHARACTERISTICS

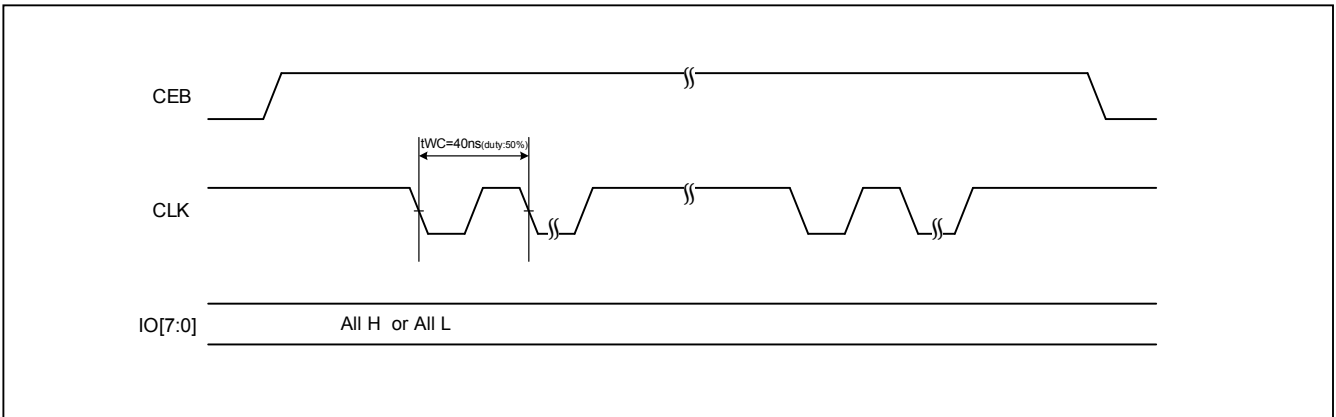
Table 7. DC Characteristics ( $T_A = 0 \sim 60^\circ\text{C}$ ,  $V_{CC} = 2.8 \sim 3.4\text{V}$ ,  $V_{CCIO} = 1.62 \sim 1.98\text{V}$ )

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	MAX.	UNIT
Input High Voltage	V <sub>IH</sub>	-		0.75 * V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-		-0.3	0.3 * V <sub>CCIO</sub>	V
Schmitt Trigger Input (L to H) (CLK, CEB)	V <sub>t+</sub>	-		-	0.7 * V <sub>CCIO</sub>	V
Schmitt Trigger Input (H to L) (CLK, CEB)	V <sub>t-</sub>	-		0.3 * V <sub>CCIO</sub>	-	V
Schmitt Trigger Hysteresis Voltage (CLK, CEB)	(delta)V <sub>t</sub>	-		0.15	-	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400uA		0.85 * V <sub>CCIO</sub>	-	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.6mA		-	0.1 * V <sub>CCIO</sub>	V
Operating Current 1	I <sub>CC</sub>	tWC=40ns		-	115	mA
Operating Current 2	I <sub>CCIO</sub>	tWC=40ns		-	20	mA
Standby Current 1-1	I <sub>CC_STB1</sub>	CEB= V <sub>CCIO</sub> - 0.2V, IO=V <sub>CCIO</sub> - 0.2V or 0.2V, CLK= V <sub>CCIO</sub> - 0.2V	T <sub>A</sub> =25°C	-	180	uA
			T <sub>A</sub> =60°C	-	300	uA
Standby Current 1-2	I <sub>CCIO_STB1</sub>	CEB= V <sub>CCIO</sub> - 0.2V, IO=V <sub>CCIO</sub> - 0.2V or 0.2V, CLK= V <sub>CCIO</sub> - 0.2V	T <sub>A</sub> =25°C	-	30	uA
			T <sub>A</sub> =60°C	-	50	uA
Standby Current 2-1	I <sub>CC_STB2</sub>	CEB= V <sub>CCIO</sub> - 0.2V, IO=V <sub>CCIO</sub> - 0.2V or 0.2V, tWC=40ns (Duty 50%)	T <sub>A</sub> =25°C	-	180	uA
			T <sub>A</sub> =60°C	-	300	uA
Standby Current 2-2	I <sub>CCIO_STB2</sub>	CEB= V <sub>CCIO</sub> - 0.2V, IO=V <sub>CCIO</sub> - 0.2V or 0.2V, tWC=40ns (Duty 50%)	T <sub>A</sub> =25°C	-	30	uA
			T <sub>A</sub> =60°C	-	50	uA
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to V <sub>CCIO</sub> (max)		-	±10	uA
Output Leakage Current	I <sub>LO</sub>	V <sub>OUT</sub> = 0 to V <sub>CCIO</sub> (max)		-	±10	uA

Note1: only happen during the 1st page read of boundary, other pages will not.



**Figure 2. Standby Current (ISTB1)**



**Figure 3. Standby Current (ISTB2)**

## 12. CAPACITANCE

Table 8. Capacitance ( $T_A = 0\sim 60^\circ\text{C}$ ,  $V_{CC} = 2.8\sim 3.4\text{V}$ ,  $V_{CCIO} = 1.62\sim 1.98\text{V}$ ,  $f = 1.0\text{MHz}$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0\text{V}$	-	10	pF
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{V}$	-	10	pF

## 13. AC CHARACTERISTICS

Table 9. AC TEST CONDITION

PARAMETER	TEST CONDITIONS
Input Pulse Level	$V_{CCIO} * 0.1$ to $V_{CCIO} * 0.9$
Input Rise and Fall Times	3ns
Input Timing Levels (CLK)	$V_{CCIO} * 0.5$
Input Timing Levels (CEB, IO, RESB)	$V_{CCIO} * 0.3$ to $V_{CCIO} * 0.7$
Output Timing Levels	0.45V to $V_{CCIO} - 0.45\text{V}$
Output Load	30pF

Note1:  $V_{CCIO} = 1.62\text{V}\sim 1.98\text{V}$

Table 10. AC Characteristics (25MHz, T<sub>A</sub> = 0~60°C, V<sub>CC</sub> = 2.8~3.4V, V<sub>CCIO</sub> = 1.62~1.98V)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
CLK Cycle Time		tWC	38	40	-	ns
CLK High Pulse Width		tWH	18	20	-	ns
CLK Low Pulse Width		tWL	18	20	-	ns
CEB Setup Time		tCS	120	-	-	ns
CEB Hold Time		tCH	165	-	-	ns
CEB High Pulse Width		tCEPH	300	-	-	ns
Data Setup Time		tDS	15	-	-	ns
Data Hold Time		tDH	4	-	-	ns
Data Valid Time		tDV	0	-	-	ns
CLK Access Time (Note3)		tREA	0	-	27	ns
Ready/Busy1	RD_ID1	tRB_N1	2			cycle
	RD_ID2	tRB_N2	2			cycle
	RD_ID3	tRB_N3	2			cycle
	CHG_INIT	tRB_N4	2			cycle
	RD_PAGE	tRB_N5	-	-	100	us
	RD_SELF_REFRESH	tRB_N6	2			cycle
	RD_REFRESH_STATUS	tRB_N7	2			cycle
	iRD_INIT	tRB_I1	-	-	200	us
	iSET_INIT1	tRB_I2	314			cycle
	iSET_GEN_RAND	tRB_I3	-	-	50	us
	iSET_INIT2	tRB_I4	314			cycle
	t1RD_ID1	tRB_S1	18	-	24	cycle
	t1RD_ID2	tRB_S2	18	-	24	cycle
	t1RD_ID3	tRB_S3	18	-	24	cycle
	t1RD_UID	tRB_S4	-	-	100	us
	t1RD_PAGE	tRB_S5	-	-	100	us
	t1RD_REFRESH	tRB_S6	26			cycle
	t1RD_SET_KEY	tRB_S7	314			cycle
Ready/Busy2	RD_PAGE	tRB2_N1	2 cycle	-	40	us
	t1RD_PAGE	tRB2_S1	2 cycle	-	40	us
CEB High to Output Hi-Z Time (Note1)		tCHZ	-	-	30	ns
Output to Hi-Z Time (Note1)		tDHZ	-	-	38	ns
Latency1		tHZ1	2			cycle
Latency2		tHZ2	1			cycle
Latency3		tHZ3	1			cycle
Active to Standby Time (Note1)		tAST	-	-	300	ns

Note1: This spec is guaranteed with design specification, not tested.

Note2: tRB\_\* and tRB2\_\* are based on Wait=0cycle.

Note3: Data always starts to output after CLK rising edge.

Table 11. AC Characteristics for RESB Timing ( $T_A = 0 \sim 60^\circ\text{C}$ ,  $V_{CC} = 2.8 \sim 3.4\text{V}$ ,  $V_{CCIO} = 1.62 \sim 1.98\text{V}$ )

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
RESB Non-Active Time	tRNA	9	-	-	us
RESB Low Time 1	tRES1	100	-	-	us
RESB High Time 1	tRH1	250	-	-	ms
RESB Setup Time	tRS	100	-	-	ns
RESB Low Time 2	tRES2	1	-	-	us
RESB High Time 2	tRH2	250	-	-	ms

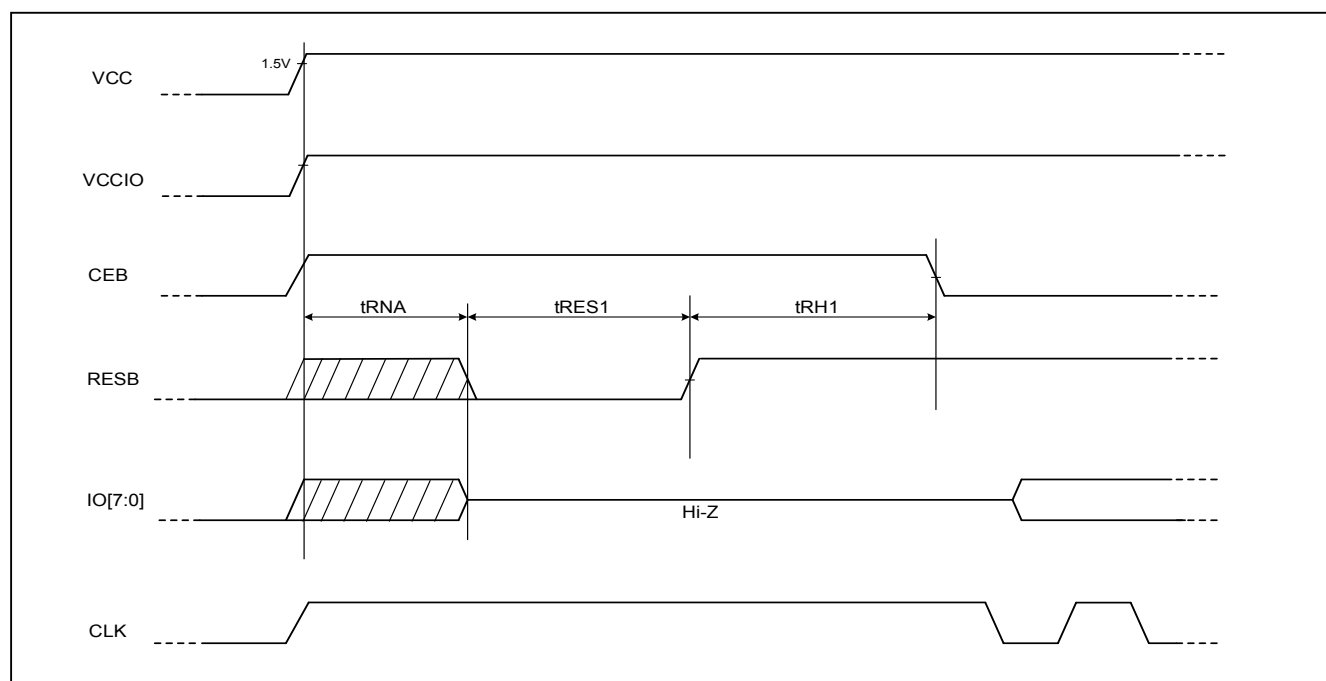
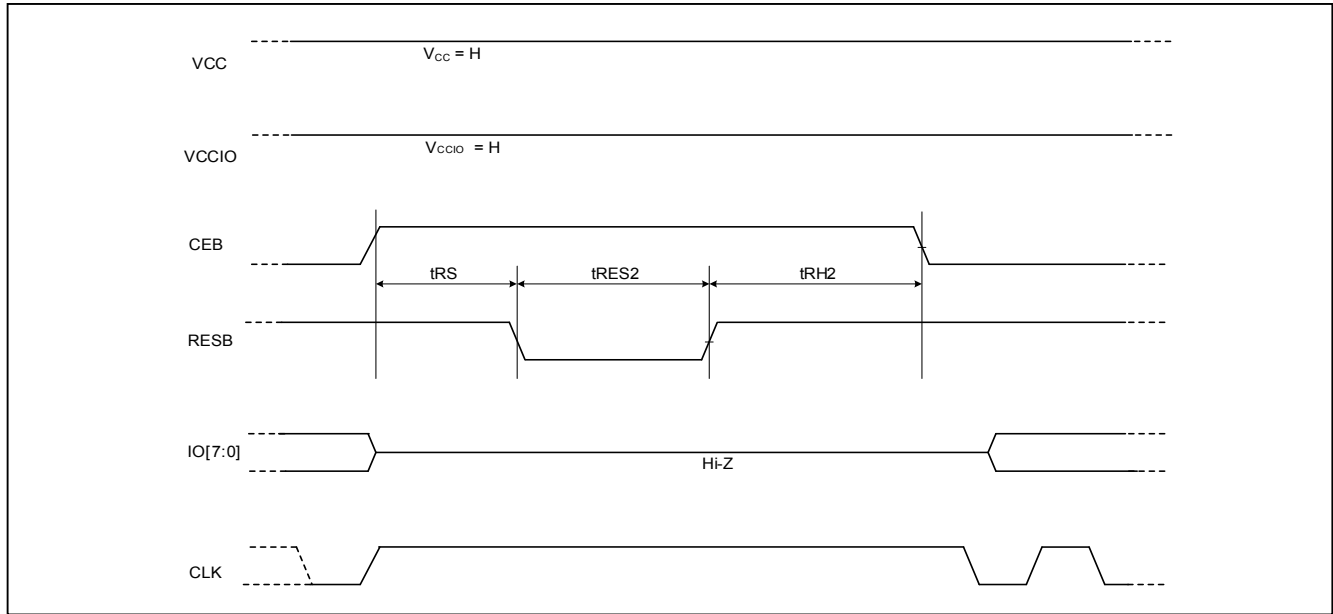


Figure 4. RESB Timing Waveform (Case1)

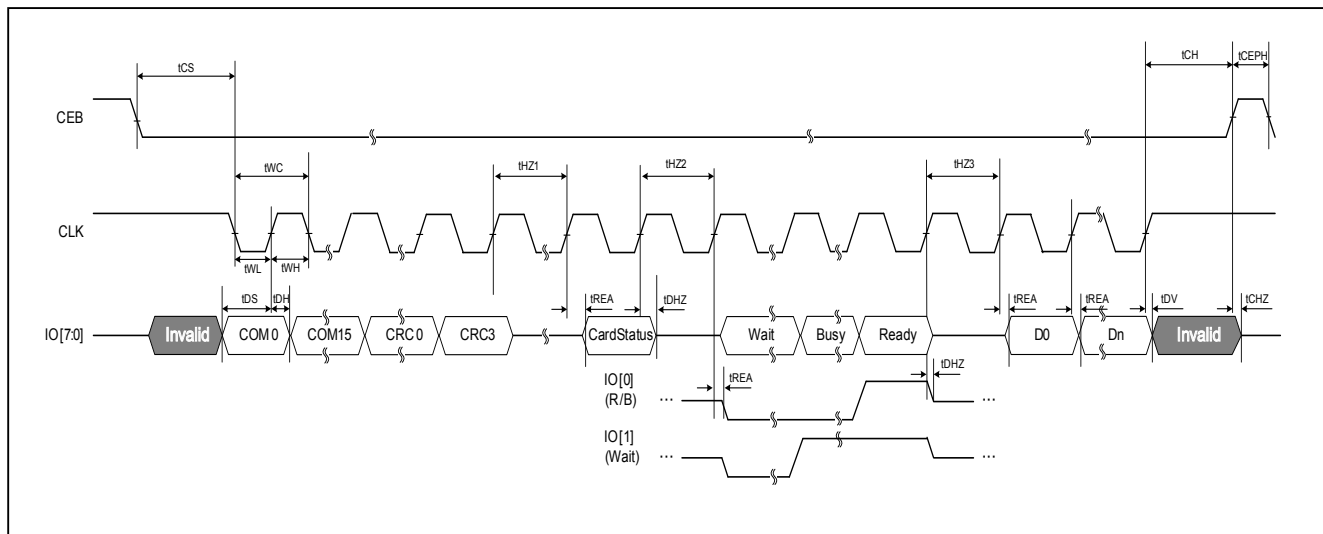
Note 1: During "RESB=L", IO7~IO0 is Hi-Z.

Note 2: RESB from low to high will triggered POR function during tRH1.

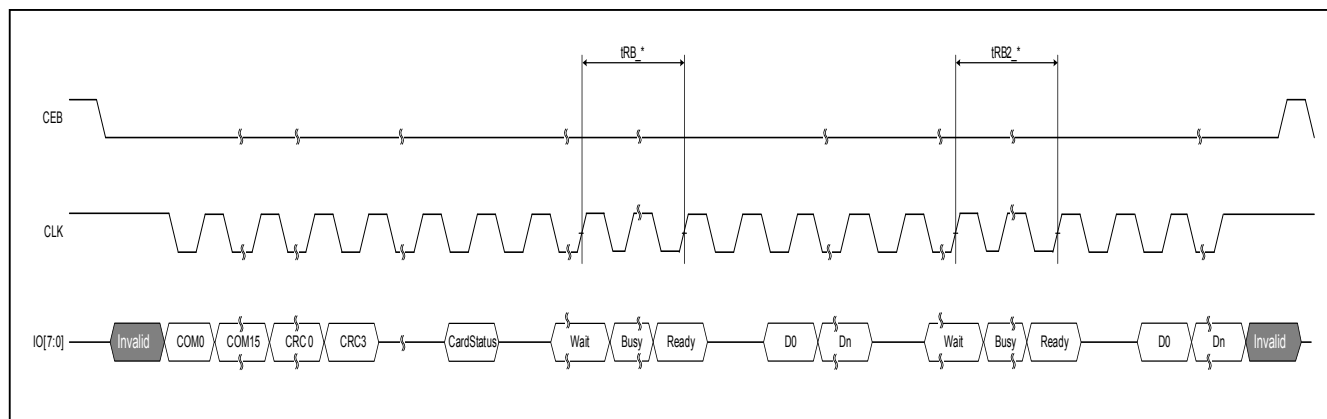


**Figure 5. RESB Timing Waveform (Case 2)**

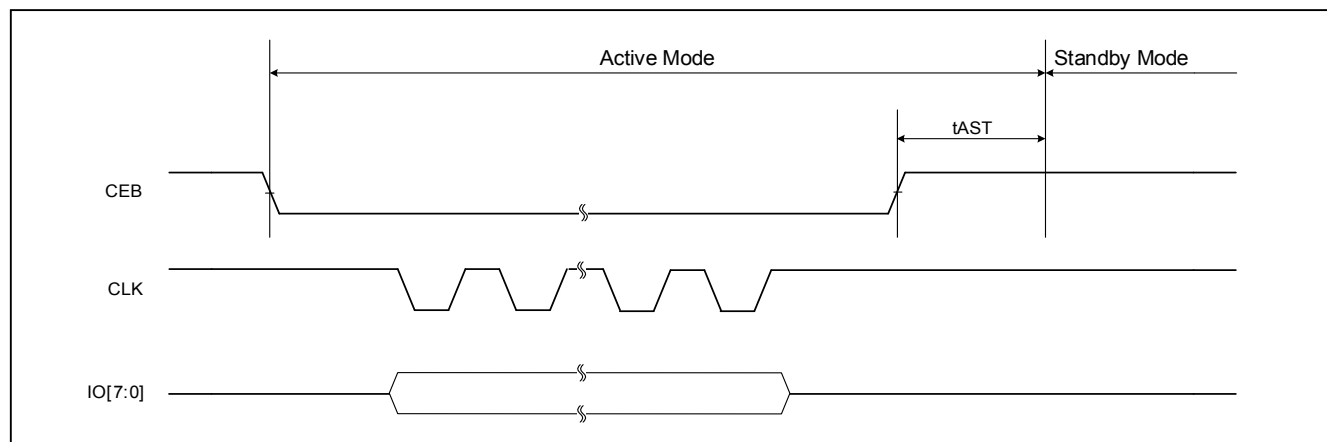




**Figure 6. Command Input and Data Output Timing Waveform (Read, 25MHz)**



**Figure 7. Ready/Busy Timing Waveform (Read, 25MHz)**



**Figure 8. Standby Mode Timing Waveform**



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#### **14. POWER SUPPLY DECOUPLING**

In order to reduce power noise, please connect 0.1uF ceramic capacitor between power (VCC and VCCIO) and ground.





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